

761GX-M754

REV:B--->1.0


REV:1.0

PCB: 15-K97-011000

BOM: 89-200-K97100

- P1.COVER SHEET
- P2.BLOCK
- 03.ClawHammer_1_HyperTransport
- 04.ClawHammer_2_DDR
- 05.ClawHammer_3_Misc
- 06.ClawHammer_4_Power
- 07.DDR DIMM
- 08.Termination Resistors
- 09.761GX-1 LDT, PCI Express
- 10.761GX-2 MuTIOL & Others
- 11.761GX-3 Power and Ground
- 12.761GX-4 Power, Decoupling
- 13.PCI Express_X16
- 14.VGA Connector
- 15.Clock Generator
- 16.964-1 PCI/IDE/HyperZip
- 17.964-2 LPC/MII/CPU/GPIO
- 18.964-3 USB/SATA
- 19.964-4 Power
- 20.PCI 1
- 21.PCI 2 & PCI3
- 22.IDE
- 23.Super I/O (ITE8712)
- 24.HM/FAN
- 25.COM1/COM2/LPT
- 26.KB/MS/ROM/FDC
- 27.ATX/Panel/RTC
- 28.USB
- 29.RT8800 (CPU VCORE)
- 30.VCC2.5VDUAL&DDR_VTT
- 31.IVDD/VDDQ
- 32.Dual/PWR_Detect
- 33.Audio Codec
- 34.Audio Interface
- 35.LANPHY(RTL8201BL/CL)

	Signature	Date
Designer	Eli Yang	10/04/2005
Layout	Ruru	
Check	Jacy Wu	
Approval	Evan	

 Elitegroup Computer Systems

Title

761GX-M754

Size

Custom

Document Number

Cover Sheet

Rev

1.0

Date:

Tuesday, October 04, 2005

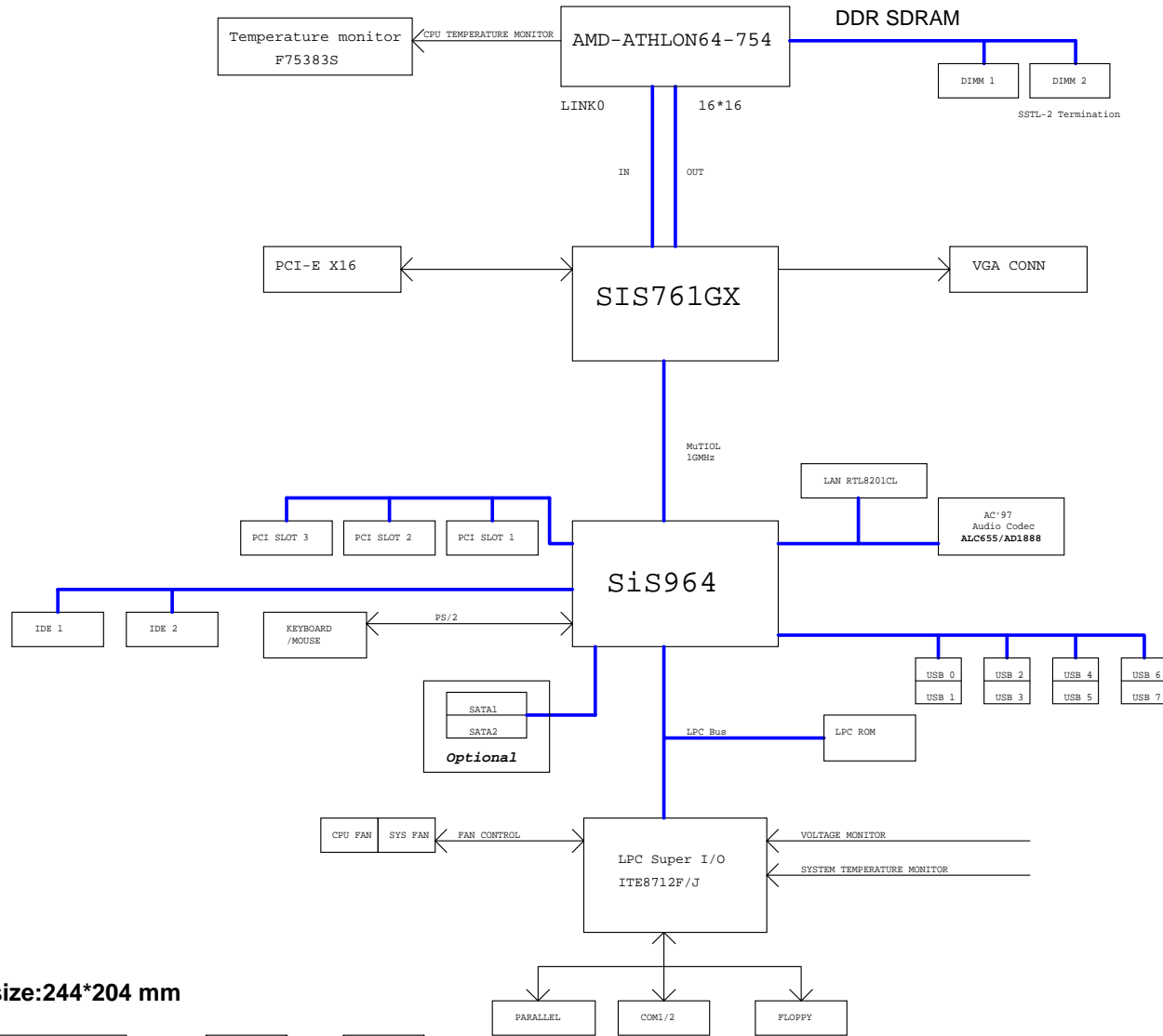
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of

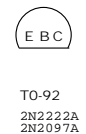
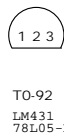
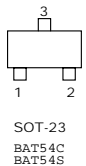
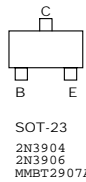
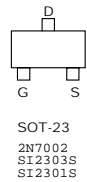
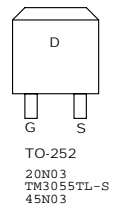
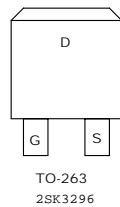
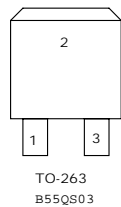
35

System Block Diagram

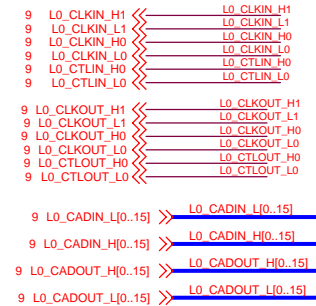
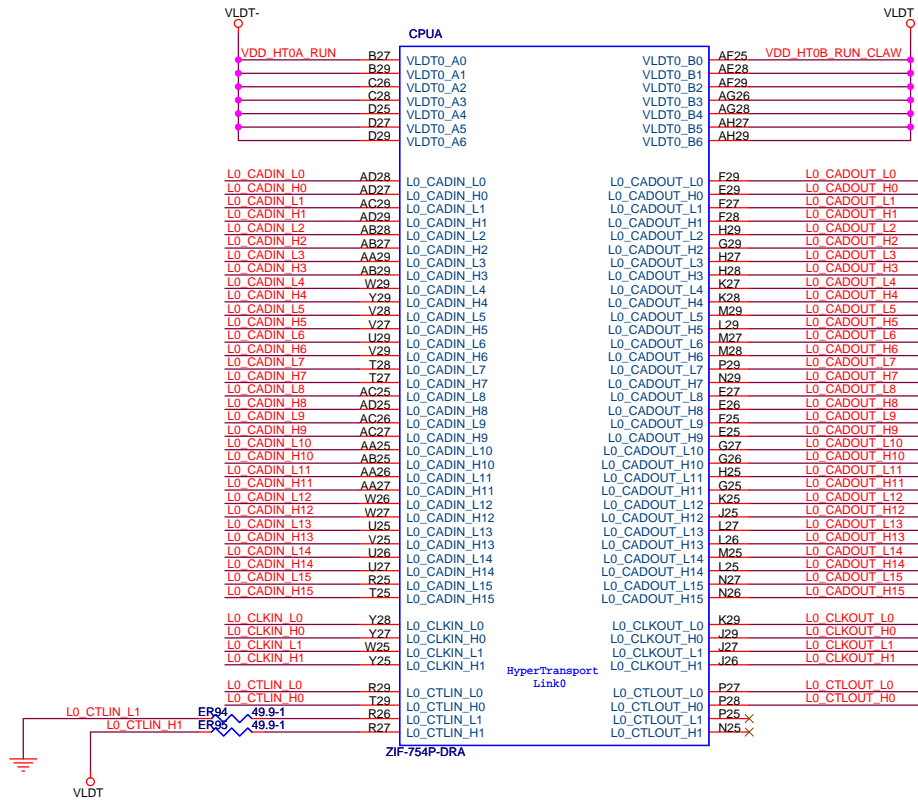


PCB size:244*204 mm

22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1200U/16DE	10*25 mm
1800U/63DE	8*20 mm
3300U/25DE	10*25 mm



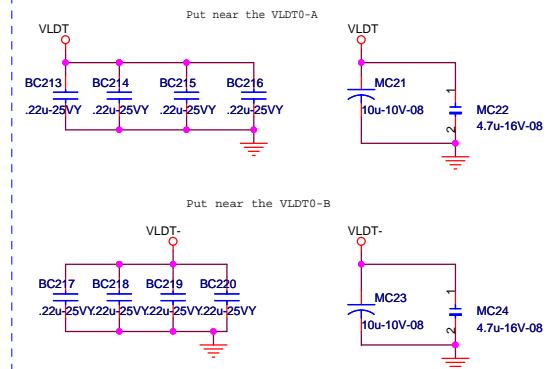
761GX-M754		
Size	Document Number	Rev
Custom	BLOCK SCH.	1.0
Date:	Tuesday, October 04, 2005	Sheet 2 of 35

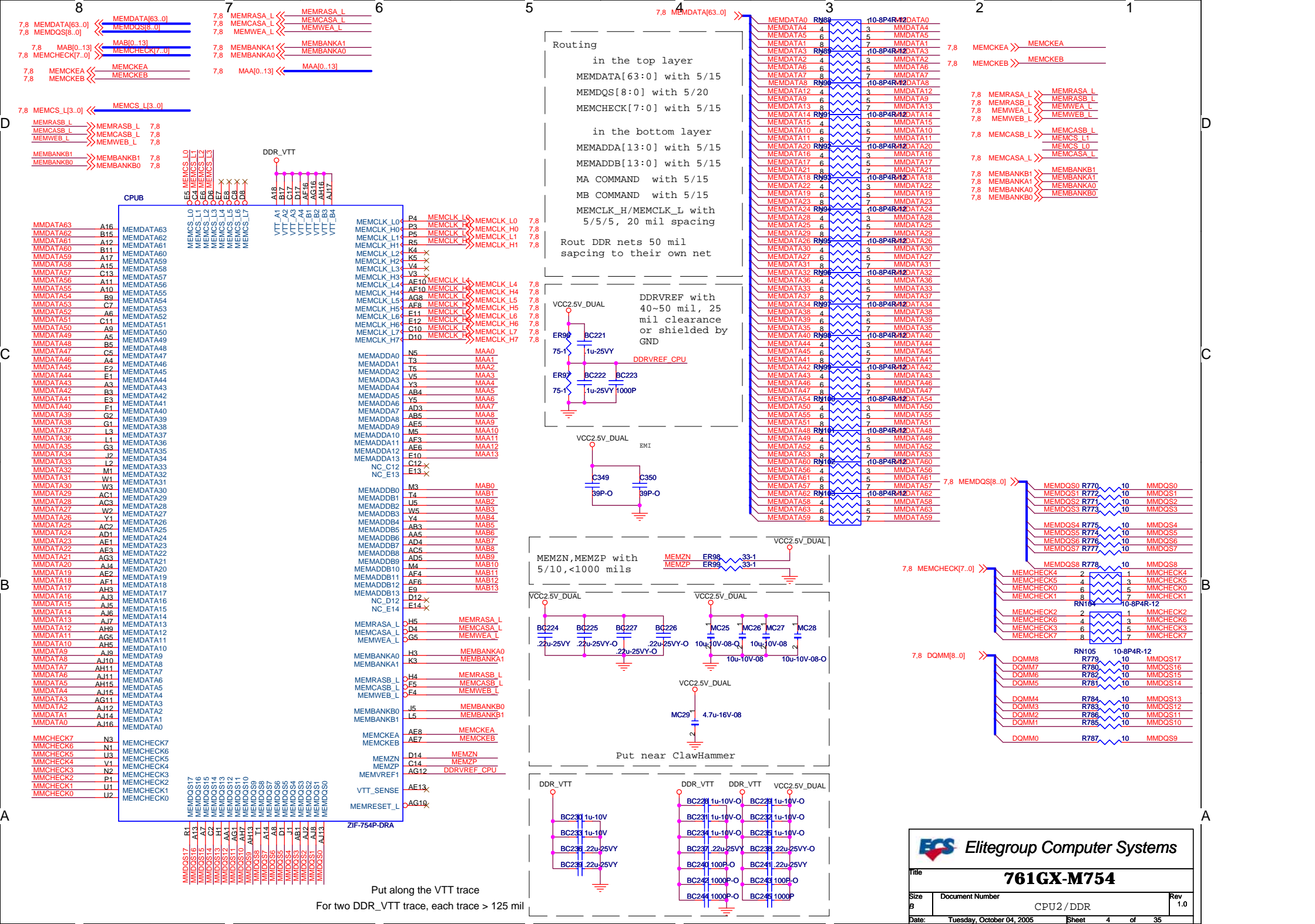


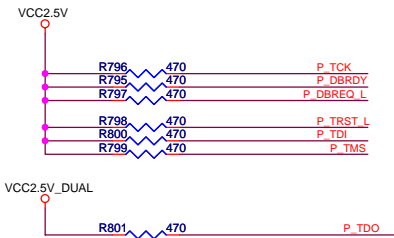
VLDT Power Decoupling

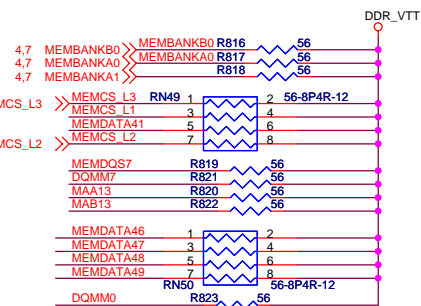
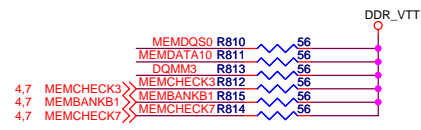
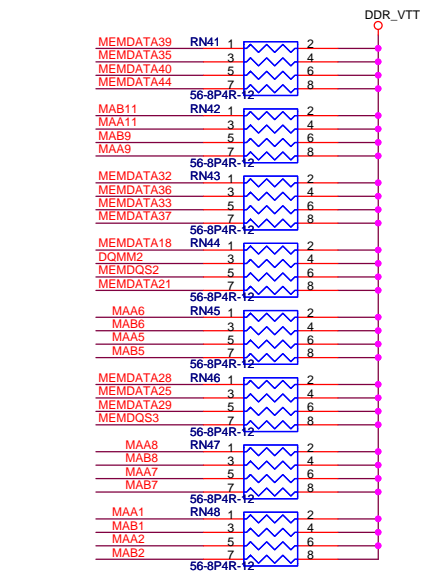
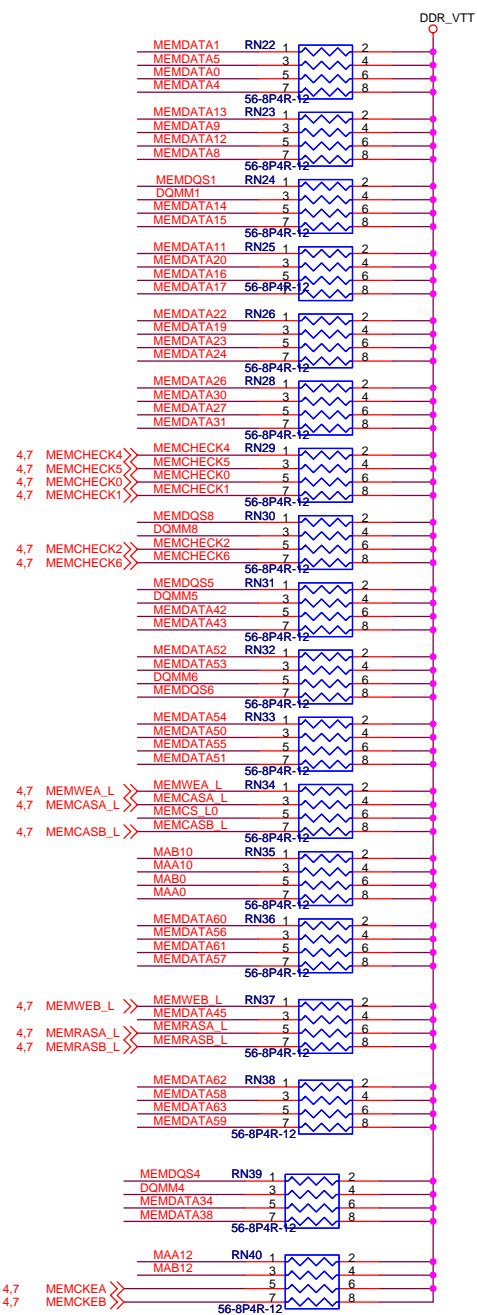
Rout with 250 mil trace or a plane

In CPU pins rout >100 mil

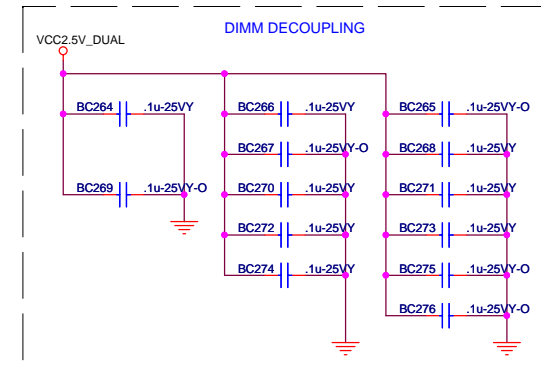
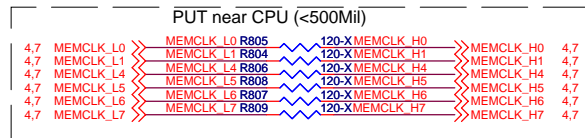
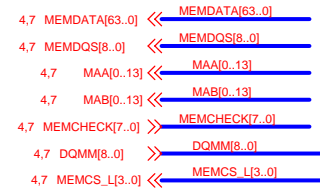
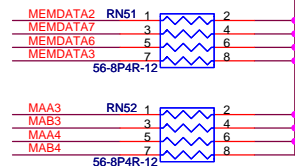
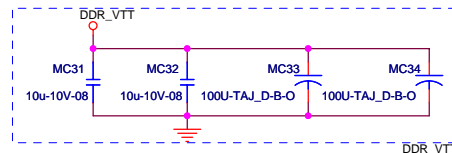






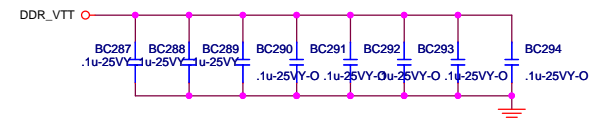
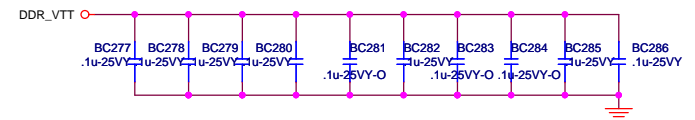


LAYOUT: Place one 1210 10uF capacitor on each end of the VTT island.

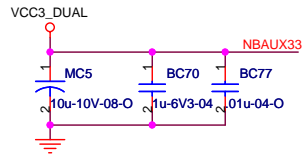


LAYOUT: Place alternating caps to GND and VCC2.5V_DUAL

in a single line along VTT island.



3 L0_CADIN_L[0..15] >> L0_CADIN_L[0..15]
3 L0_CADIN_H[0..15] >> L0_CADIN_H[0..15]
3 L0_CADOUT_H[0..15] >> L0_CADOUT_H[0..15]
3 L0_CADOUT_L[0..15] >> L0_CADOUT_L[0..15]



L0_CADOUT_H0 AE32
L0_CADOUT_H1 AD34
L0_CADOUT_H2 AB32
L0_CADOUT_H3 AA34
L0_CADOUT_H4 V34
L0_CADOUT_H5 T32
L0_CADOUT_H6 R34
L0_CADOUT_H7 N32
L0_CADOUT_H8 AC30
L0_CADOUT_H9 AB29
L0_CADOUT_H10 Y30
L0_CADOUT_H11 U30
L0_CADOUT_H12 T29
L0_CADOUT_H13 N30
L0_CADOUT_H14 N29
L0_CADOUT_H15 L30
L0_CADOUT_L0 AD32
L0_CADOUT_L1 AC34
L0_CADOUT_L2 AA32
L0_CADOUT_L3 Y34
L0_CADOUT_L4 U34
L0_CADOUT_L5 R32
L0_CADOUT_L6 P34
L0_CADOUT_L7 M32
L0_CADOUT_L8 AC31
L0_CADOUT_L9 AA29
L0_CADOUT_L10 Y31
L0_CADOUT_L11 U31
L0_CADOUT_L12 R29
L0_CADOUT_L13 P31
L0_CADOUT_L14 M29
L0_CADOUT_L15 L31

LDT_TX

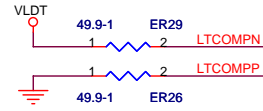
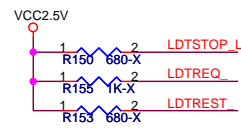
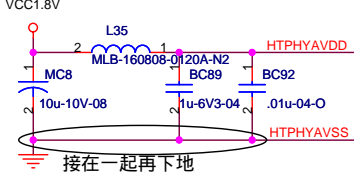
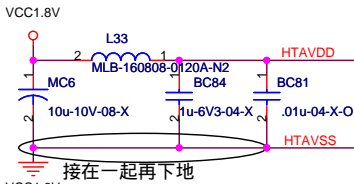
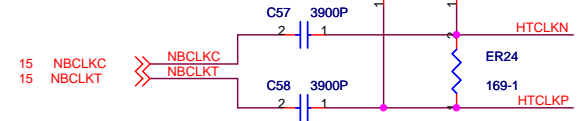
LDT_RX

756/761GX-1

PCI Express_TX

PCI Express_RX

3 L0_CLKIN_L0 >> L0_CLKIN_L0
3 L0_CLKIN_H0 >> L0_CLKIN_H0
3 L0_CLKIN_L1 >> L0_CLKIN_L1
3 L0_CLKIN_H1 >> L0_CLKIN_H1
3 L0_CTLIN_L0 >> L0_CTLIN_L0
3 L0_CTLIN_H0 >> L0_CTLIN_H0

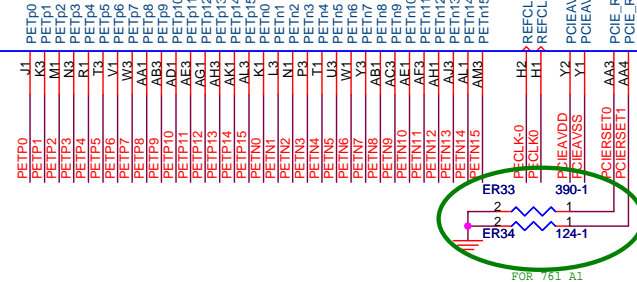


L0_CLKOUT_L0 >> L0_CLKOUT_L0
3 L0_CLKOUT_H0 >> L0_CLKOUT_H0
3 L0_CLKOUT_L1 >> L0_CLKOUT_L1
3 L0_CLKOUT_H1 >> L0_CLKOUT_H1
3 L0_CTLOUT_L0 >> L0_CTLOUT_L0
3 L0_CTLOUT_H0 >> L0_CTLOUT_H0
HTCLKN C18
HTCLKP B18
HTAVDD C17
HTAVSS A18
HTPHYAVDD A17
HTPHYAVSS B17
LDTSTOP_L F18
LDTREQ D18
LDTREST E18

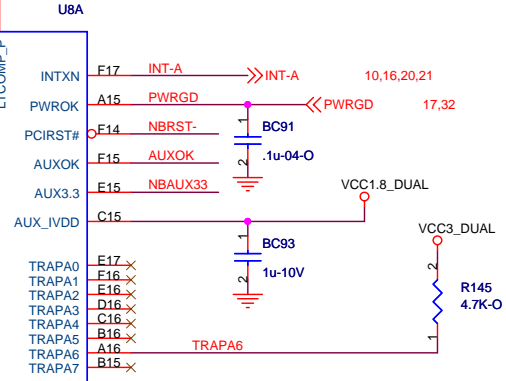
13 PETP[0..15] << PETP[0..15]
13 PETN[0..15] << PETN[0..15]
15 PECLK0 >> PECLK0
15 PECLK-0 >> PECLK-0

L0_CADIN_L0 A23
L0_CADIN_L1 A24
L0_CADIN_L2 A26
L0_CADIN_L3 A27
L0_CADIN_L4 A28
L0_CADIN_L5 A29
L0_CADIN_L6 A30
L0_CADIN_L7 A31
L0_CADIN_L8 A32
L0_CADIN_L9 A33
L0_CADIN_L10 A34
L0_CADIN_L11 A35
L0_CADIN_L12 A36
L0_CADIN_L13 A37
L0_CADIN_L14 A38
L0_CADIN_L15 A39
L0_CADIN_H0 A40
L0_CADIN_H1 A41
L0_CADIN_H2 A42
L0_CADIN_H3 A43
L0_CADIN_H4 A44
L0_CADIN_H5 A45
L0_CADIN_H6 A46
L0_CADIN_H7 A47
L0_CADIN_H8 A48
L0_CADIN_H9 A49
L0_CADIN_H10 A50
L0_CADIN_H11 A51
L0_CADIN_H12 A52
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L0_CADIN_H14 A54
L0_CADIN_H15 A55
L0_CLKIN_L0 A23
L0_CLKIN_L1 A24
L0_CLKIN_L2 A26
L0_CLKIN_L3 A27
L0_CLKIN_L4 A28
L0_CLKIN_L5 A29
L0_CLKIN_L6 A30
L0_CLKIN_L7 A31
L0_CLKIN_L8 A32
L0_CLKIN_L9 A33
L0_CLKIN_L10 A34
L0_CLKIN_L11 A35
L0_CLKIN_L12 A36
L0_CLKIN_L13 A37
L0_CLKIN_L14 A38
L0_CLKIN_L15 A39
L0_CTLIN_L0 A40
L0_CTLIN_L1 A41
L0_CTLIN_L2 A42
L0_CTLIN_L3 A43
L0_CTLIN_L4 A44
L0_CTLIN_L5 A45
L0_CTLIN_L6 A46
L0_CTLIN_L7 A47
L0_CTLIN_L8 A48
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L0_CTLIN_H0 A40
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L0_CTLIN_H2 A42
L0_CTLIN_H3 A43
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L0_CTLIN_H9 A49
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L0_CTLIN_H15 A55

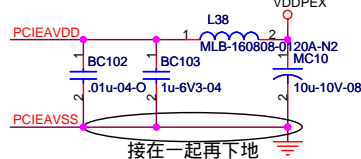
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L0_CADIN_L6 A30
L0_CADIN_L7 A31
L0_CADIN_L8 A32
L0_CADIN_L9 A33
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L0_CADIN_H0 A40
L0_CADIN_H1 A41
L0_CADIN_H2 A42
L0_CADIN_H3 A43
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L0_CADIN_H5 A45
L0_CADIN_H6 A46
L0_CADIN_H7 A47
L0_CADIN_H8 A48
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L0_CLKIN_L0 A23
L0_CLKIN_L1 A24
L0_CLKIN_L2 A26
L0_CLKIN_L3 A27
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L0_CLKIN_L5 A29
L0_CLKIN_L6 A30
L0_CLKIN_L7 A31
L0_CLKIN_L8 A32
L0_CLKIN_L9 A33
L0_CLKIN_L10 A34
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L0_CTLIN_H12 A52
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L0_CTLIN_H15 A55



NBRST- << NBRST- 16
AUXOK << AUXOK 17,27



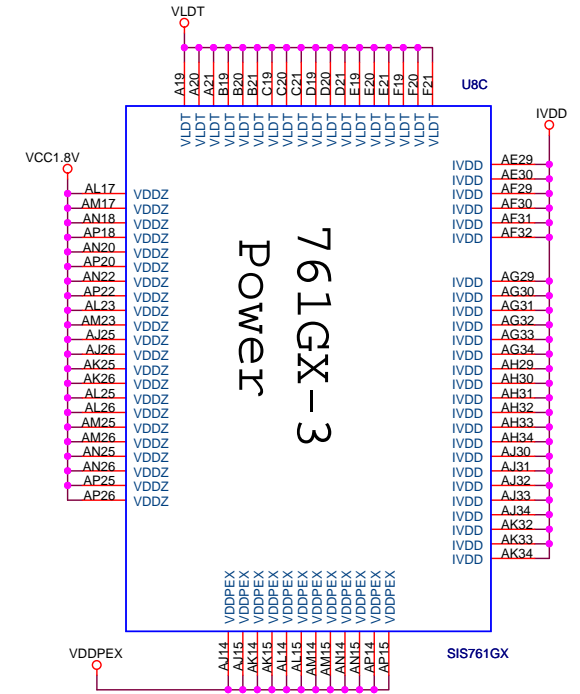
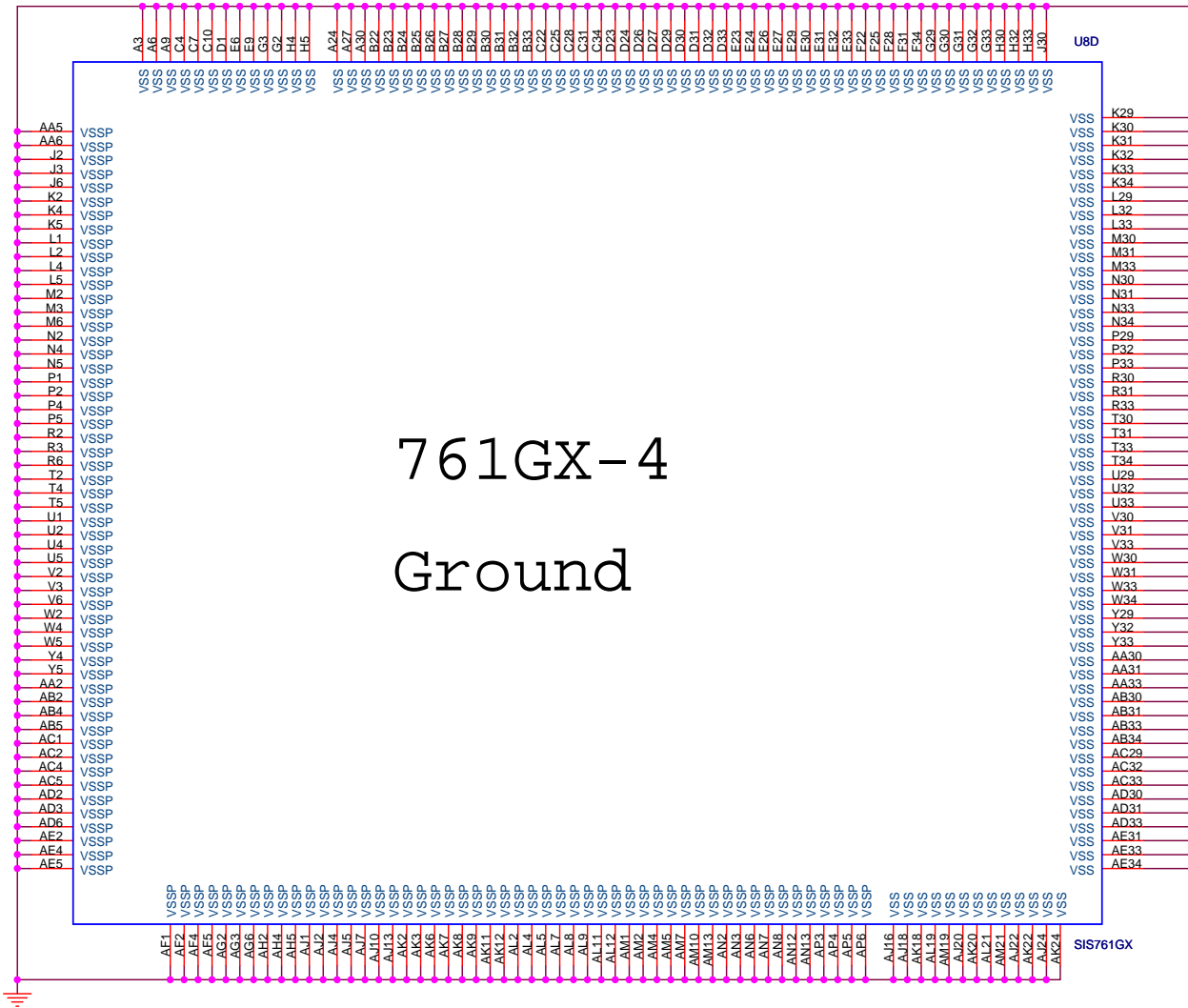
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PERP2 M5
PERP3 N6
PERP4 R5
PERP5 T6
PERP6 V6
PERP7 W6
PERP8 AB6
PERP9 AD5
PERP10 AE6
PERP11 AG5
PERP12 AH6
PERP13 AK5
PERP14 AL6
PERP15 AN5
PERN0 J4
PERN1 L6
PERN2 M4
PERN3 P6
PERN4 R4
PERN5 U6
PERN6 V4
PERN7 Y6
PERN8 AC6
PERN9 AD4
PERN10 AE6
PERN11 AG4
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PERPI0..15 << PERPI0..15 13
PERNI0..15 << PERNI0..15 13

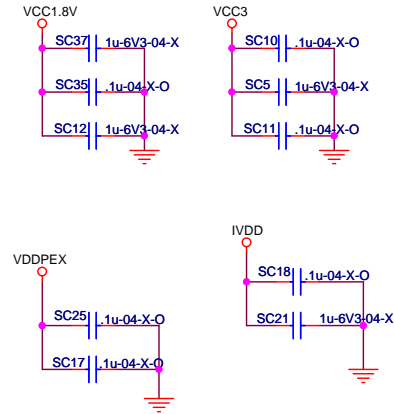
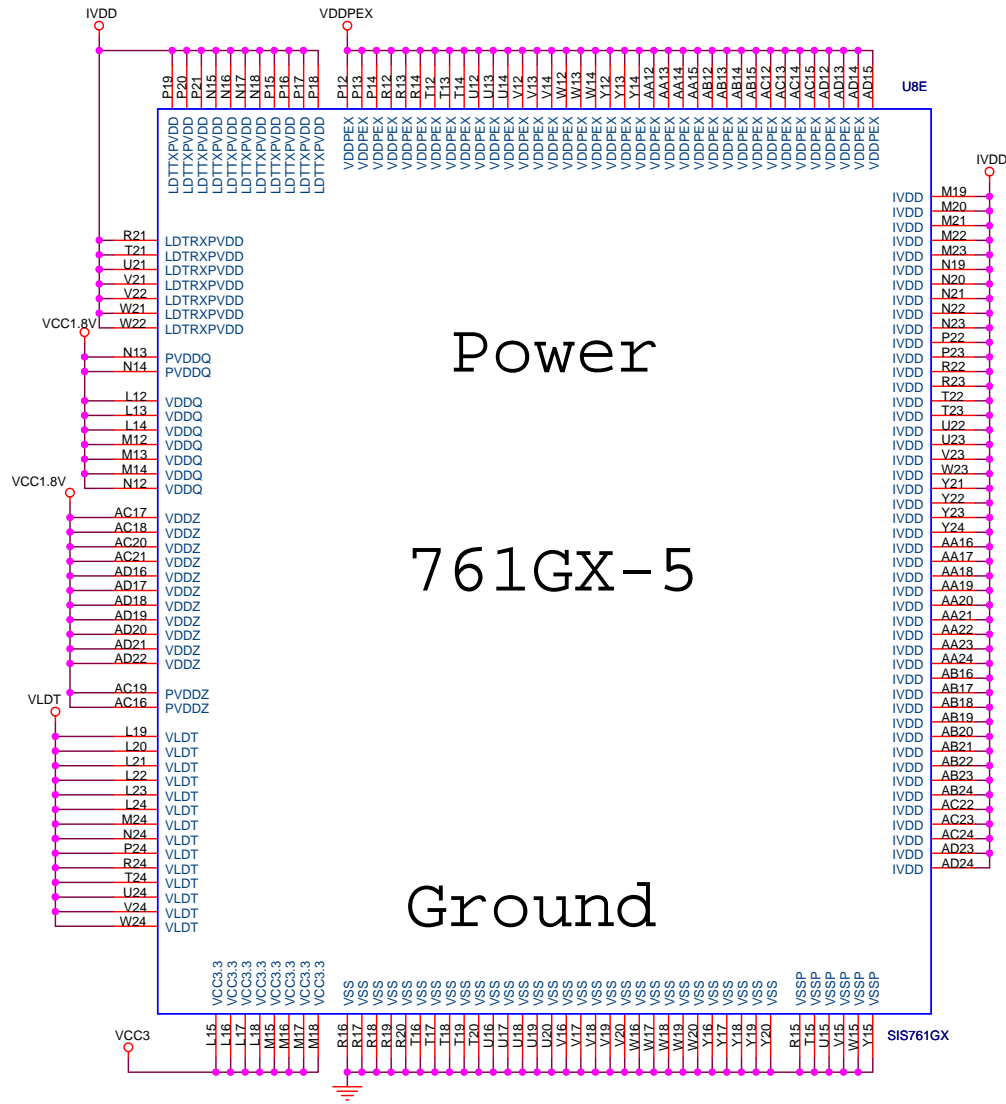


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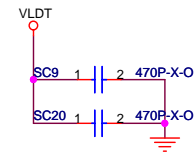
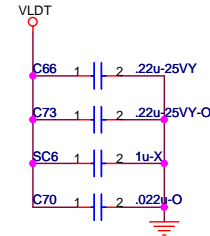
Size B	Document Number	Rev 1.0
756/761GX-1 LDT, PCI Express		
Date: Tuesday, October 04, 2005	Sheet 9 of 35	

761GX-4 Ground

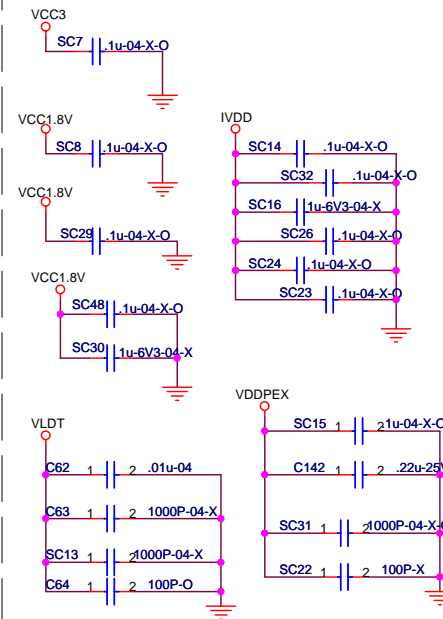




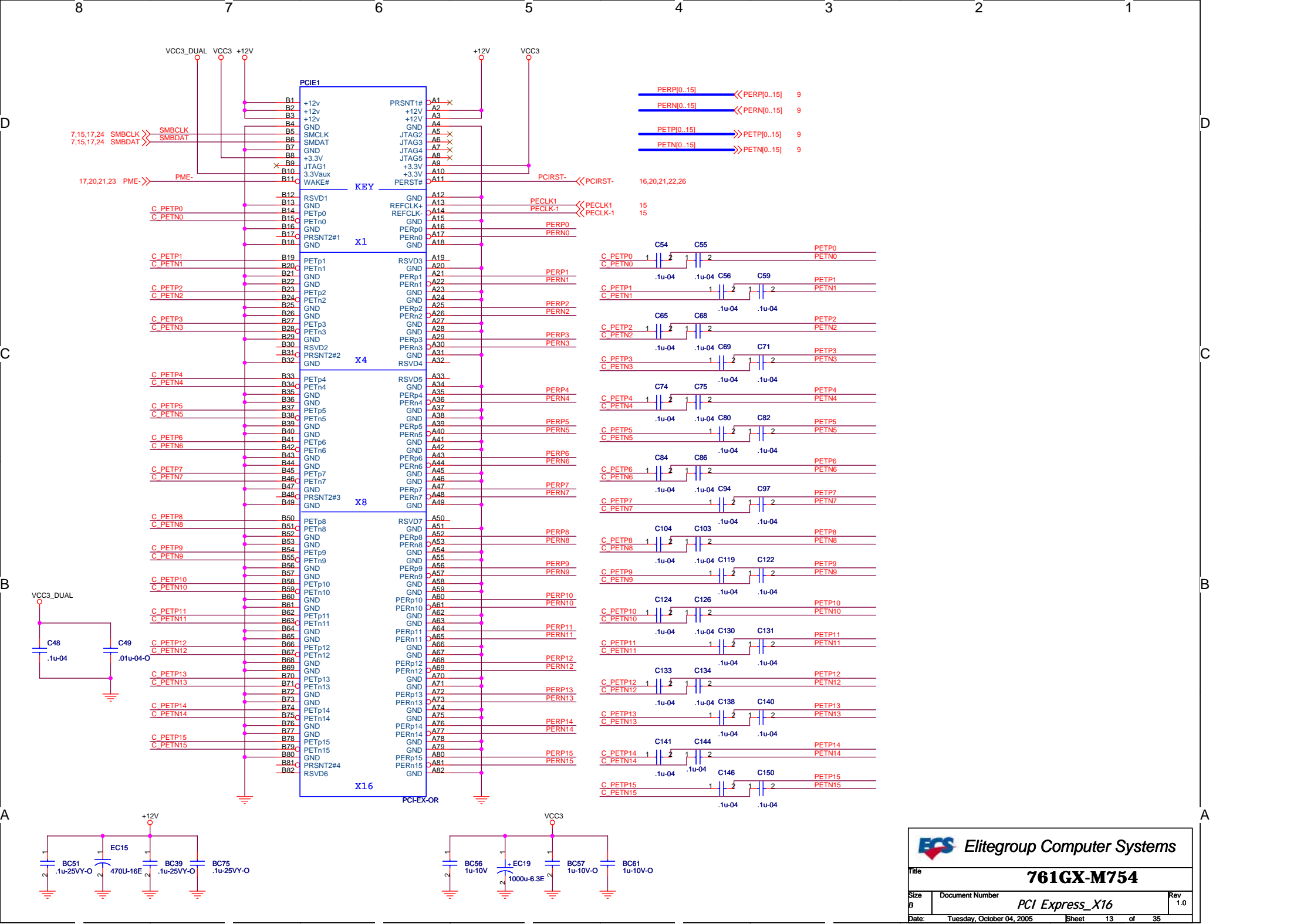
LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.

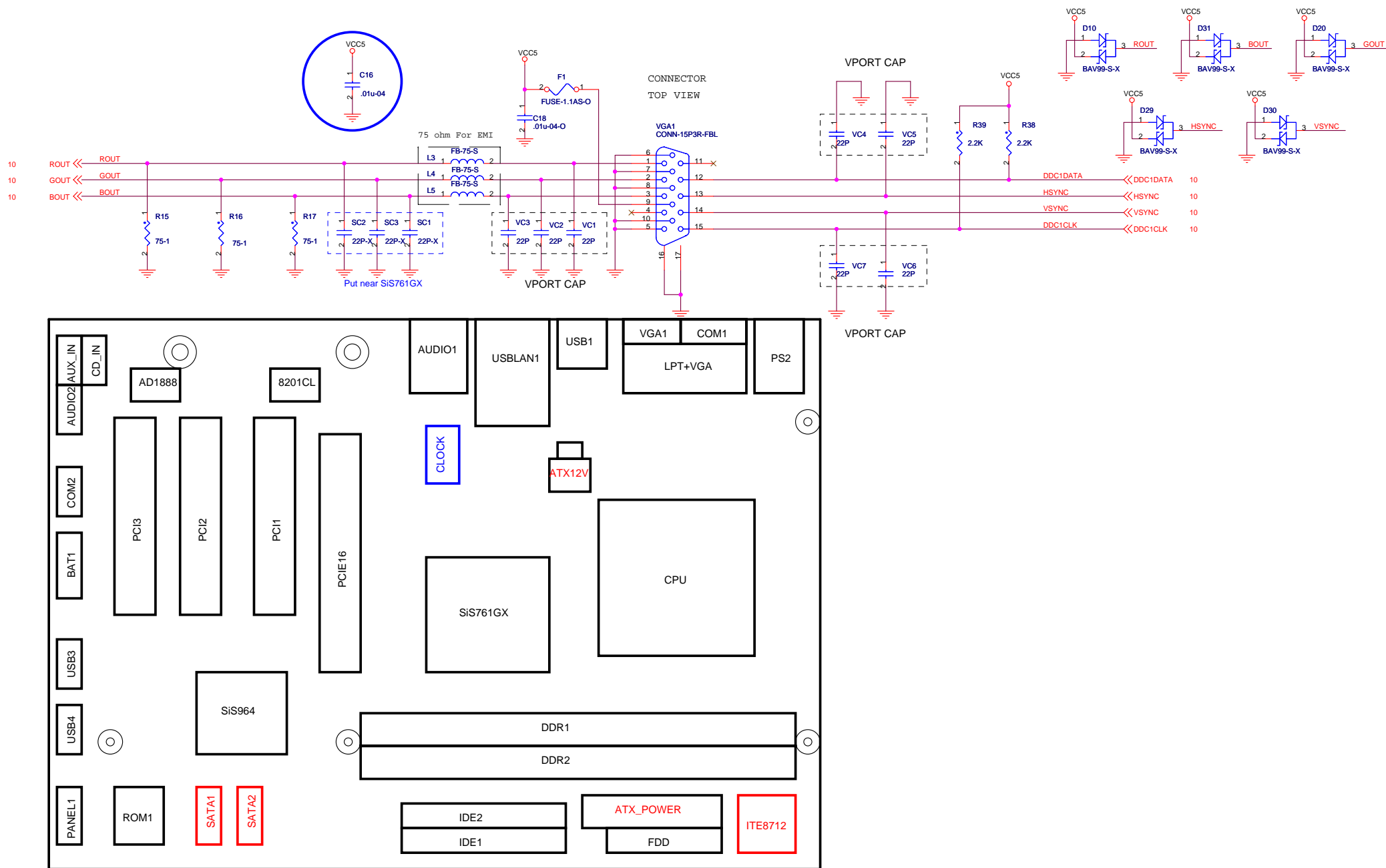


Place these capacitors under NB solder side.



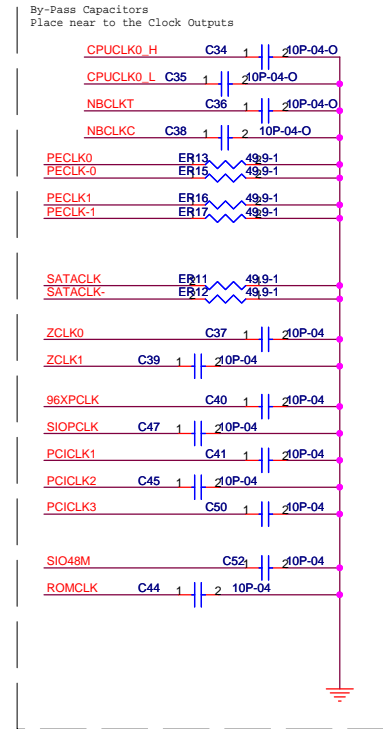
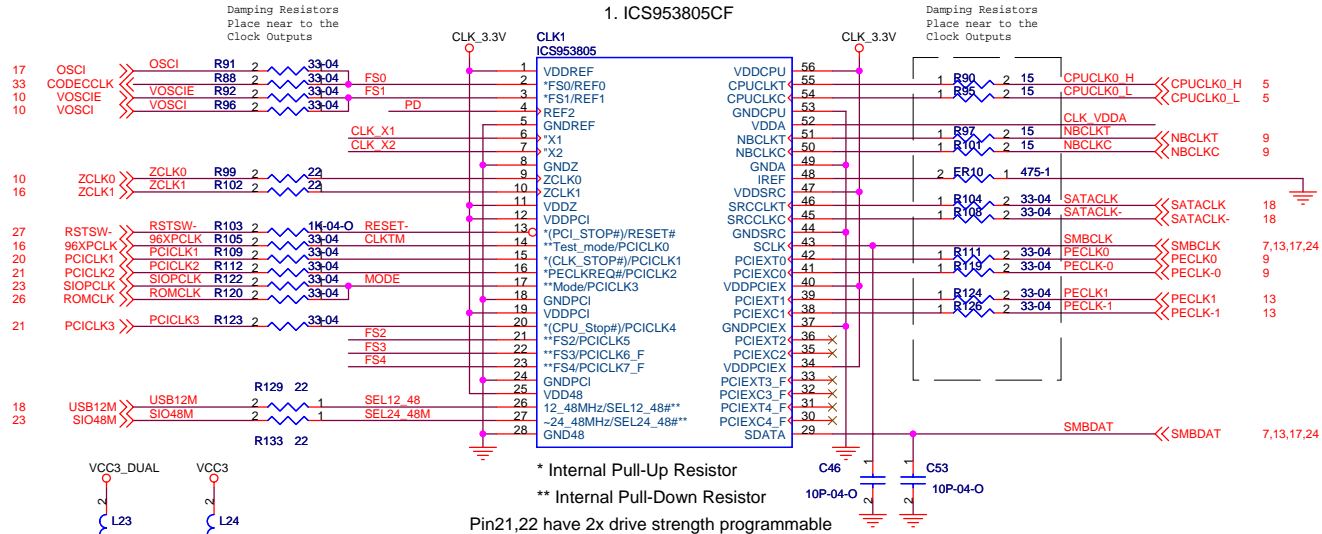
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B	761GX-4 Power, Decoupling	1.0	
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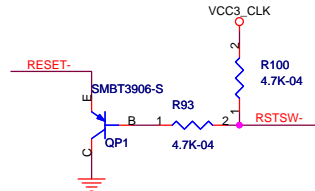
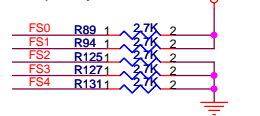


Main Clock Generator

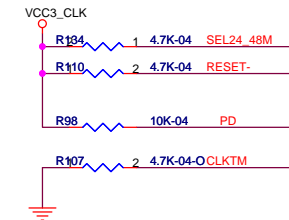
1. ICS953805CF



Frequency Selection

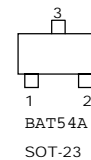


SEL24_48M 1: 24MHz
0: 48MHz
USB12M 0: 12MHz
1: 48MHz
CLKTM 1: ZCLK=66MHz
0: ZCLK=133MHz



Different clock generator with different frequency define table

SIS 756 CLOCK (ICS953801)											SIS 756 CLOCK (ICS953801)										
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPULCLK (MHz)	NBCLK (MHz)	SRC (MHz)	ZCLK (MHz)	PEI-EX (MHz)	PCI (MHz)	(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPULCLK (MHz)	NBCLK (MHz)	SRC (MHz)	ZCLK (MHz)	PCI-EX (MHz)	PCI (MHz)
0	0	0	0	0	100.00	100.00	100.00	133.33	100.00	33.33	1	0	0	0	0	133.33	166.66	100.00	133.33	100.00	33.33
0	0	0	0	1	133.33	133.33	100.00	133.33	100.00	33.33	1	0	0	0	1	166.66	222.22	100.00	133.33	100.00	33.33
0	0	0	1	0	166.66	166.66	100.00	133.33	100.00	33.33	1	0	0	1	0	200.00	250.00	100.00	133.33	100.00	33.33
0	0	0	1	1	200.00	200.00	100.00	133.33	100.00	33.33	1	0	0	1	1	250.00	333.33	100.00	133.33	100.00	33.33
0	0	1	0	0	250.00	250.00	100.00	133.33	100.00	33.33	1	0	1	0	0	266.66	400.00	100.00	133.33	100.00	33.33
0	0	1	0	1	266.66	266.66	100.00	133.33	100.00	33.33	1	0	1	1	0	333.33	500.00	100.00	133.33	100.00	33.33
0	0	1	1	0	333.33	333.33	100.00	133.33	100.00	33.33	1	0	1	1	1	400.00	500.00	100.00	133.33	100.00	33.33
0	0	1	1	1	400.00	400.00	100.00	133.33	100.00	33.33	1	0	1	1	1	466.66	566.66	100.00	133.33	100.00	33.33
0	1	0	0	0	100.00	125.00	100.00	133.33	100.00	33.33	1	1	0	0	0	202.00	202.00	100.00	134.66	101.00	33.66
0	1	0	0	1	133.33	166.66	100.00	133.33	100.00	33.33	1	1	0	0	1	252.50	252.50	100.00	134.66	101.00	33.66
0	1	0	1	0	166.66	222.22	100.00	133.33	100.00	33.33	1	1	0	1	0	336.66	336.66	100.00	134.66	101.00	33.66
0	1	0	1	1	200.00	250.00	100.00	133.33	100.00	33.33	1	1	0	1	1	468.33	468.33	100.00	134.66	101.00	33.66
0	1	1	0	0	250.00	333.33	100.00	133.33	100.00	33.33	1	1	1	0	0	202.00	252.50	100.00	134.66	101.00	33.66
0	1	1	0	1	266.66	400.00	100.00	133.33	100.00	33.33	1	1	1	1	0	252.50	336.66	100.00	134.66	101.00	33.66
0	1	1	1	0	333.33	500.00	100.00	133.33	100.00	33.33	1	1	1	1	1	336.66	466.66	100.00	134.66	101.00	33.66
0	1	1	1	1	400.00	500.00	100.00	133.33	100.00	33.33	1	1	1	1	1	400.00	500.00	100.00	134.66	101.00	33.66



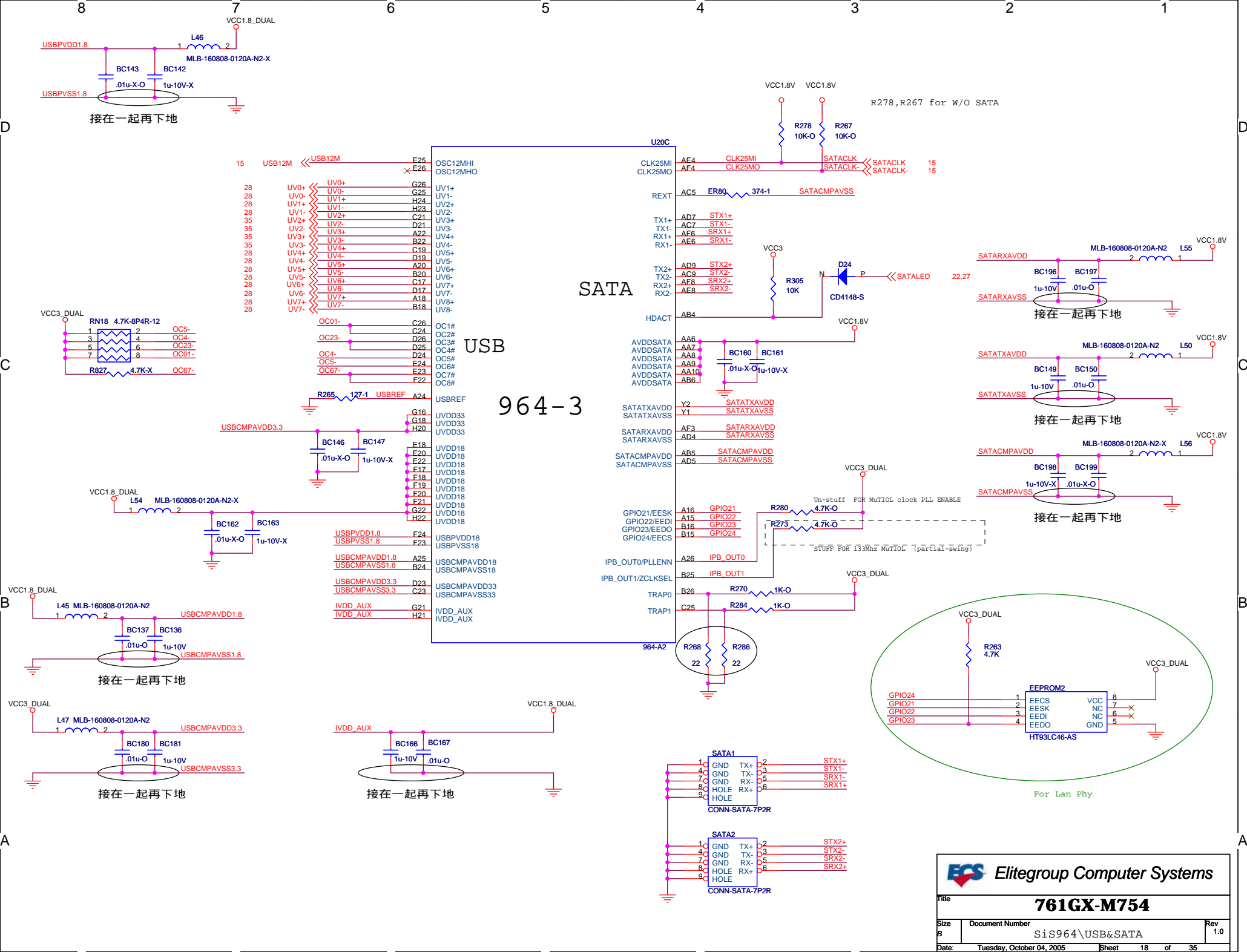
Elitegroup Computer Systems

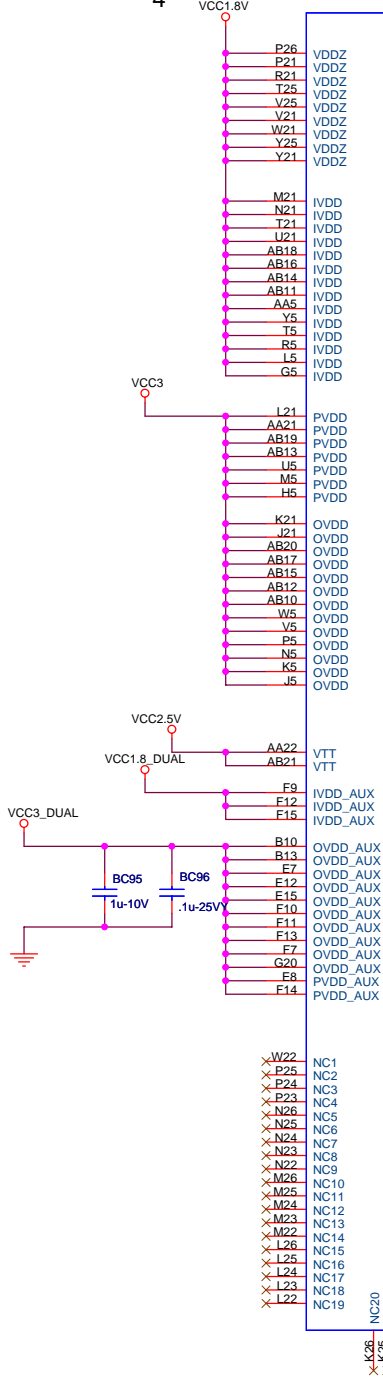
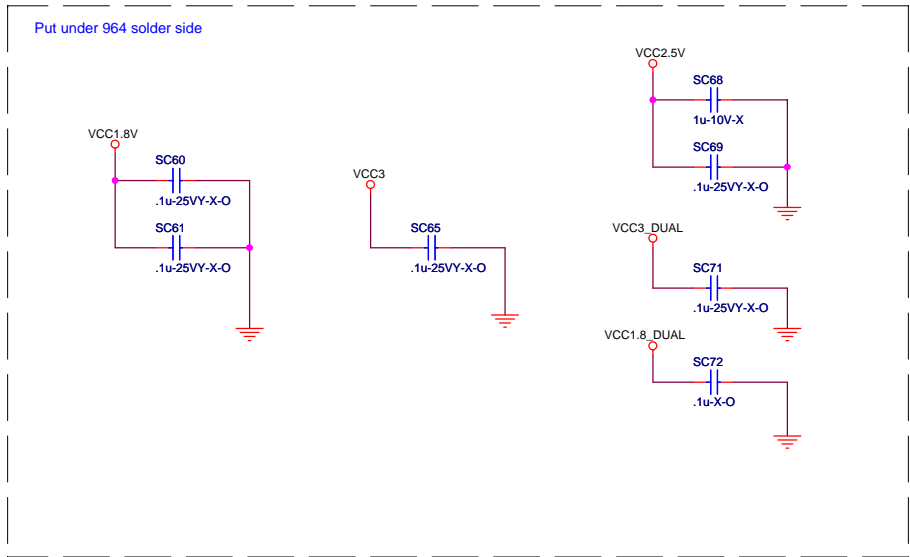
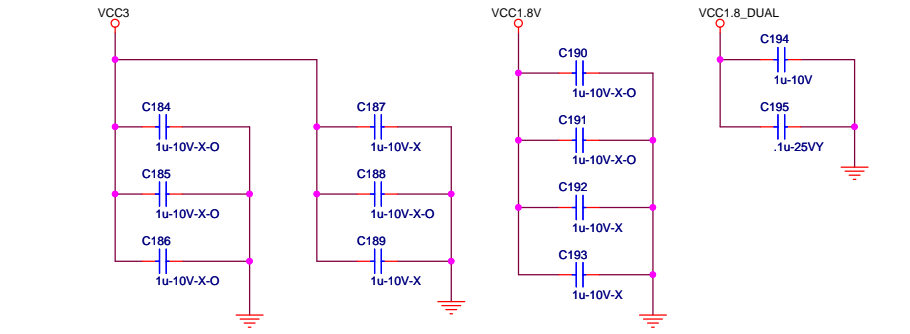
761GX-M754

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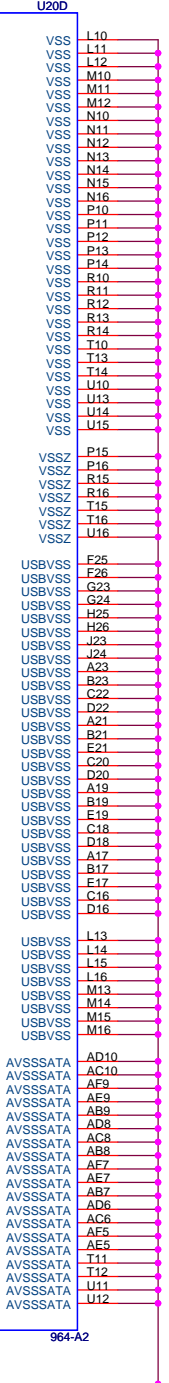
Date: Tuesday, October 04, 2005Sheet 15 of 35

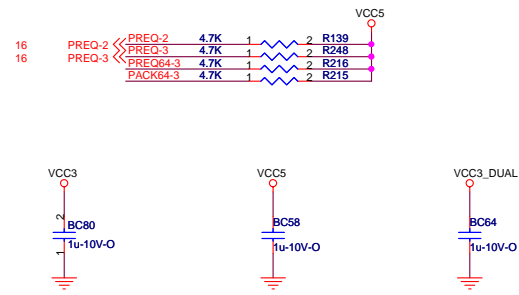
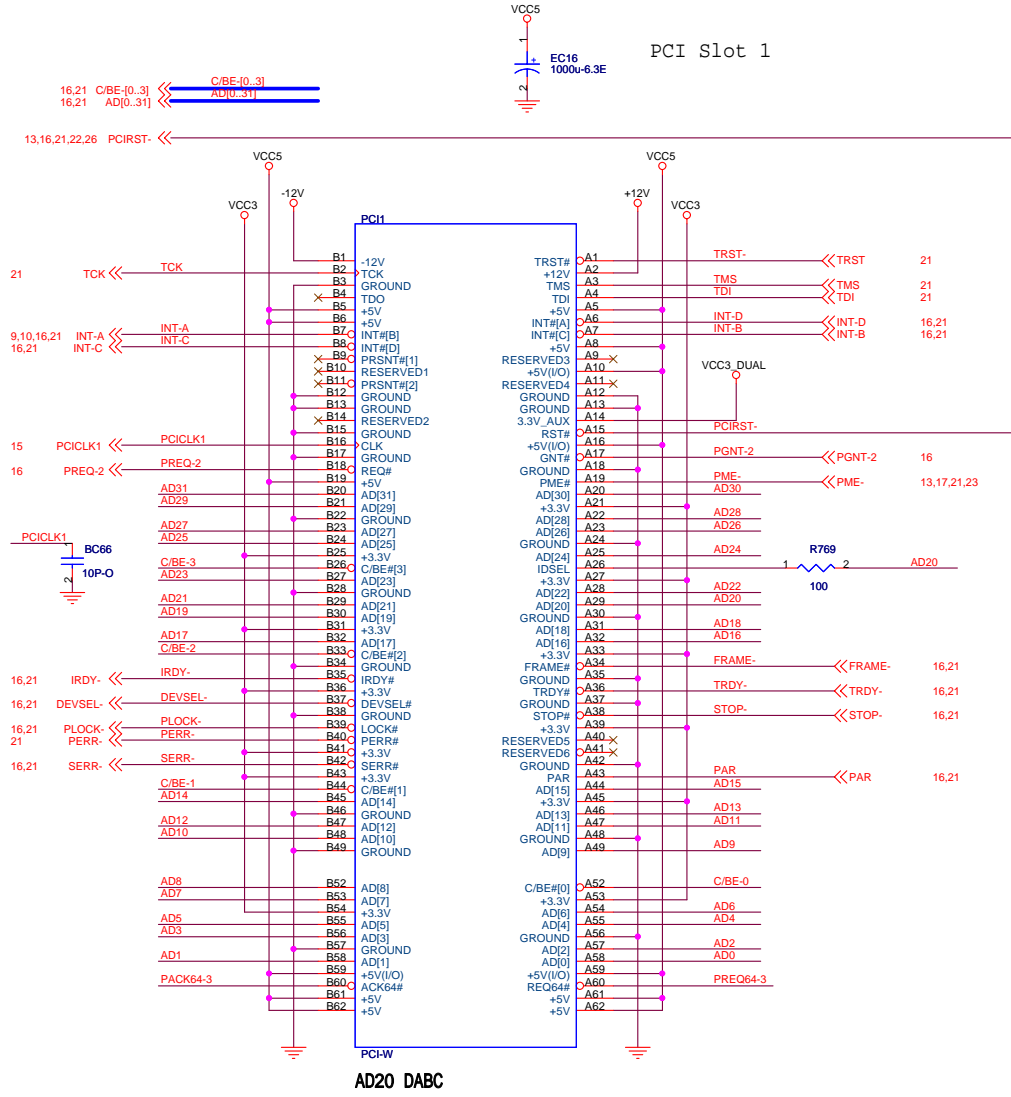


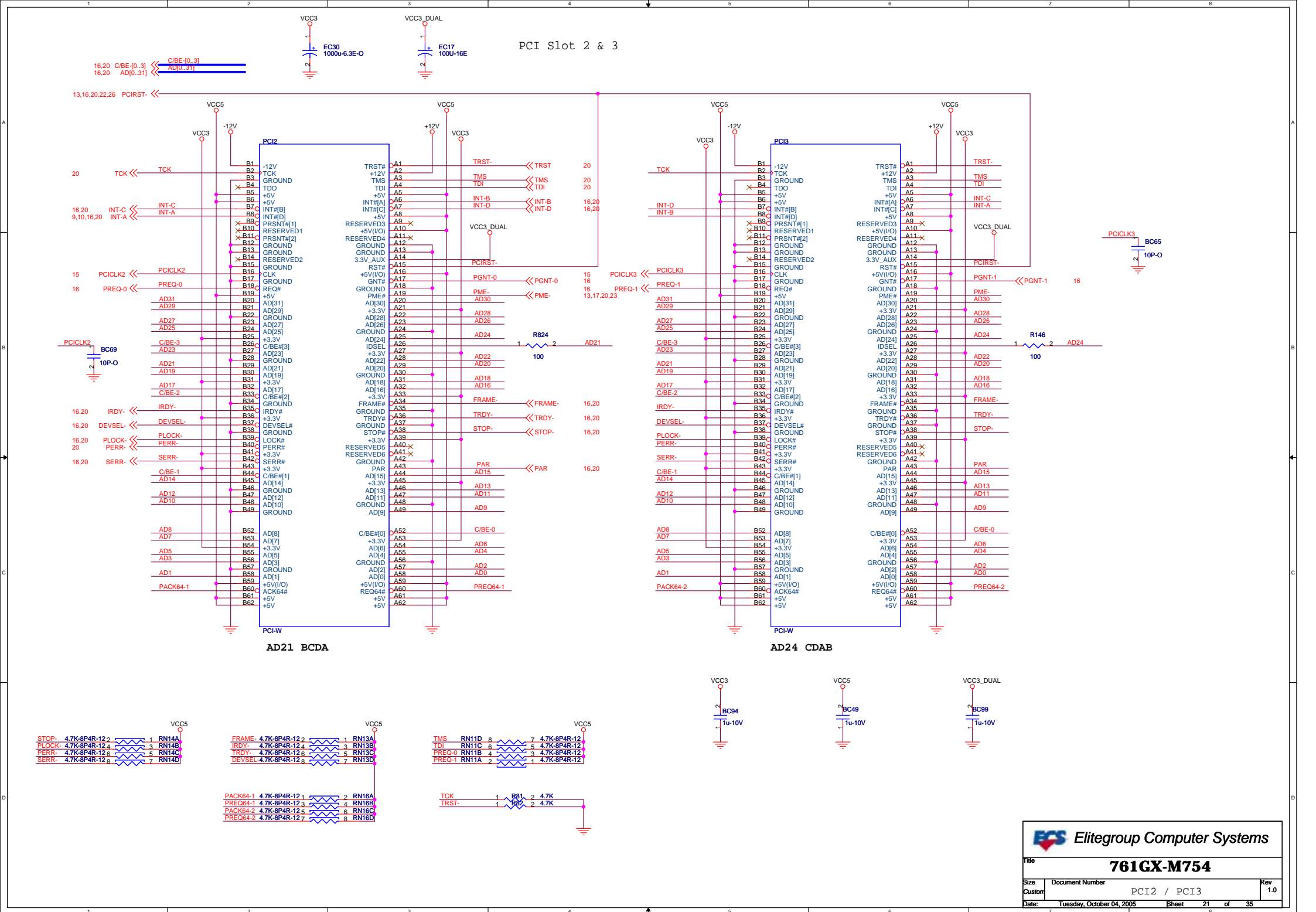




964-4
Power





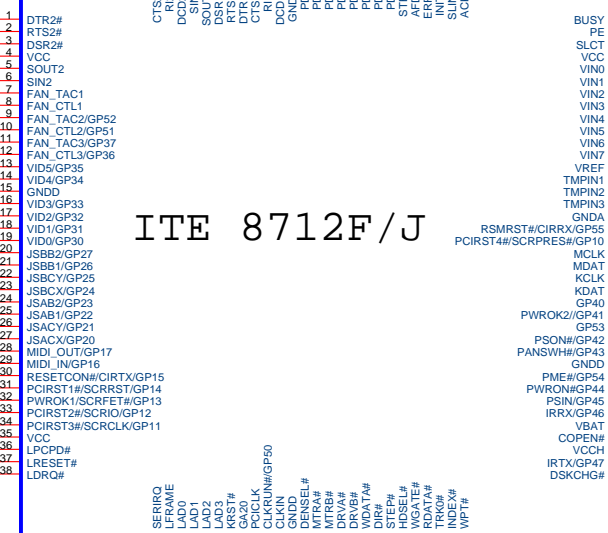


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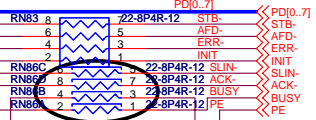
DCD-A
RI-A
CTS-A
DTR-A
RTS-A
DSR-A
SOUTA
SINA
DCD-B
RI-B
CTS-B

DCD-A
RI-A
CTS-A
DTR-A
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DSR-A
SOUTA
SINA
DCD-B
RI-B
CTS-B

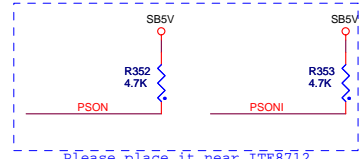
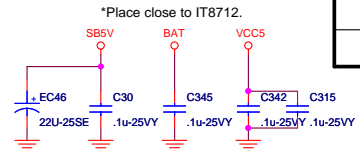
U22



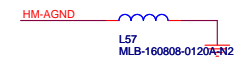
ITE 8712F/J



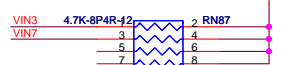
		High	Low
GPIO62	BootBlockProtect	Disable	Enable



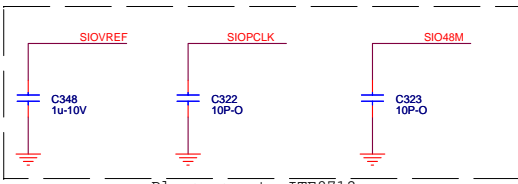
Please place it near ITE8712.



ITE 8712 POWER ON TRAPS



*Recommended net "VCCH" minimum trace width 12mils.



Place near to ITE8712

CAD Guideline: Clock signal should has 20mil spacing. PCI_RST# 20mil spacing.
PCI_RST# 20mil spacing. LAD[8:0] 5mil between eachother and 10 mil from other singnal.

Elitegroup Computer Systems

Title

761GX-M754

Size

Document Number

Super I/O (ITE8712)

Rev

1.0

Date:

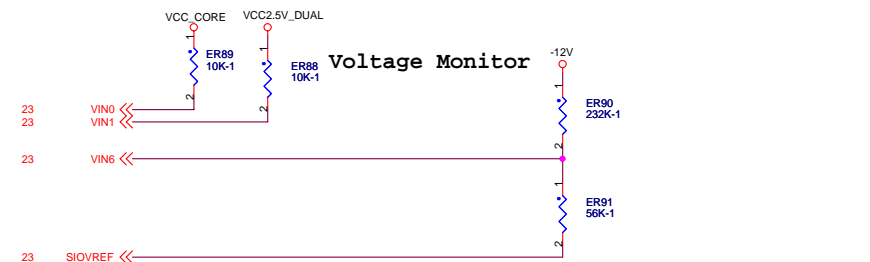
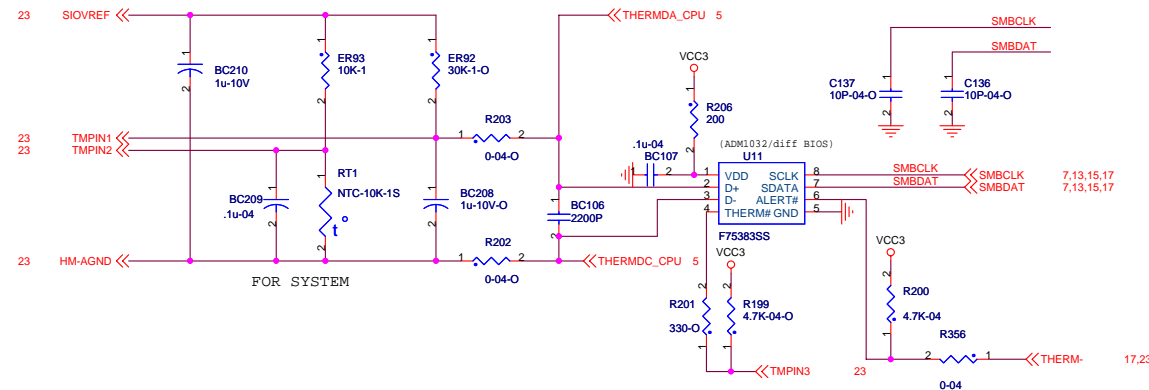
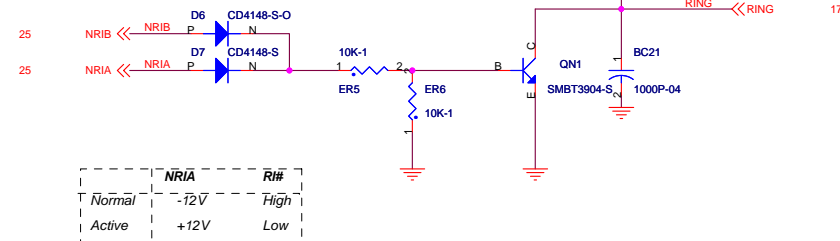
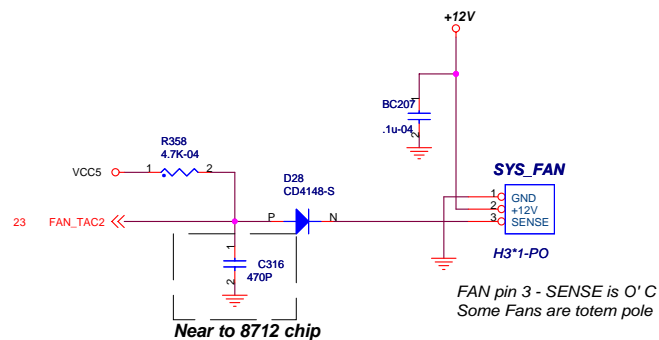
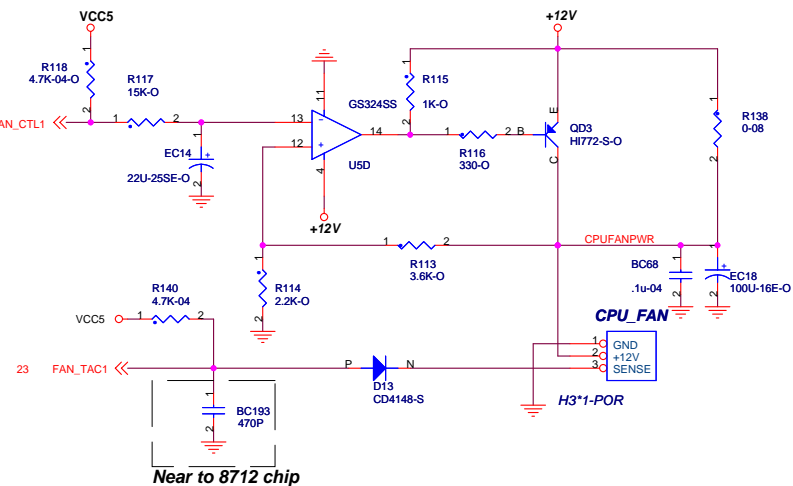
Tuesday, October 04, 2005

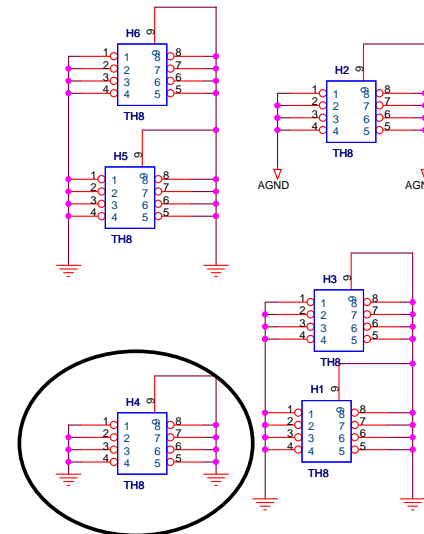
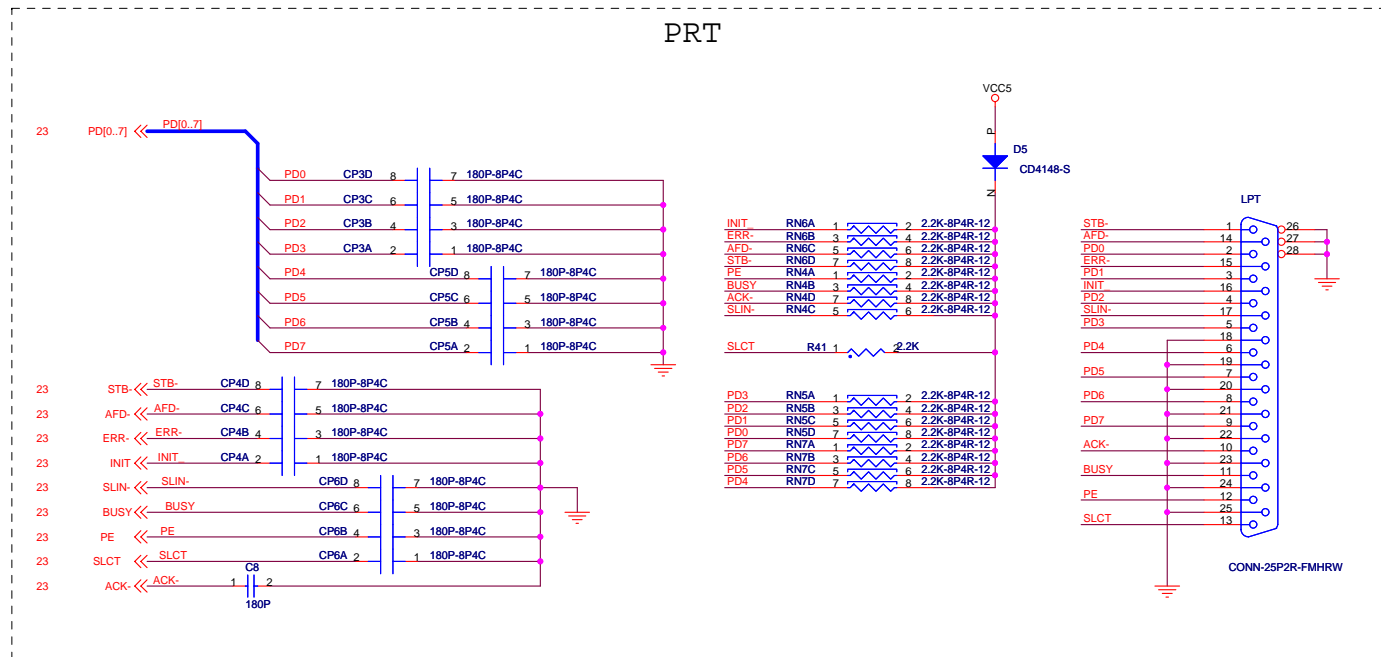
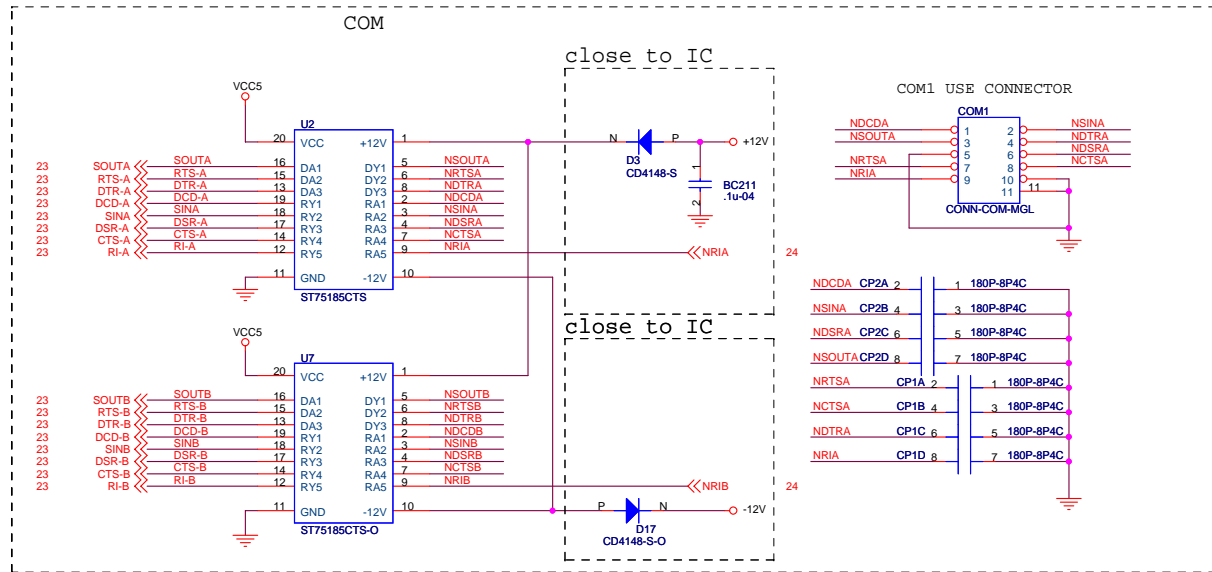
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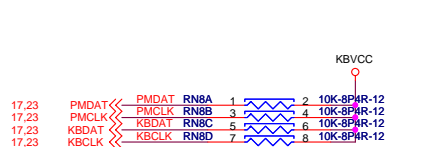
23

of

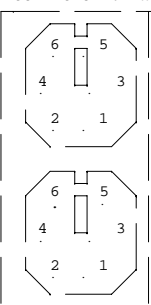
35



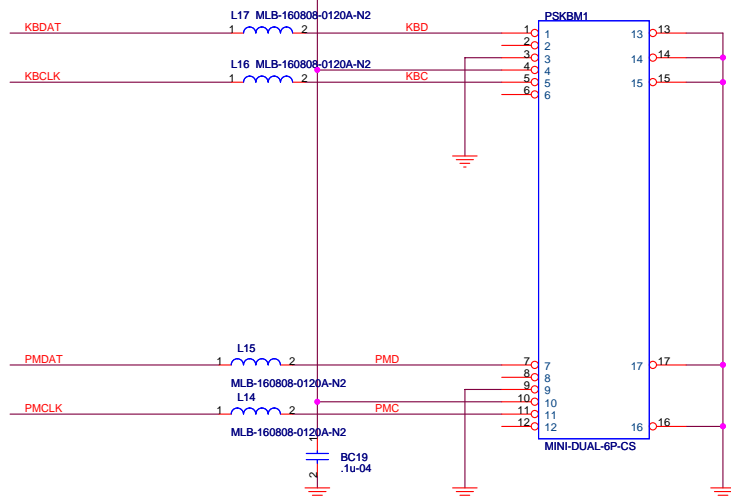
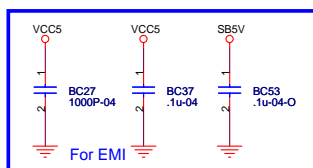
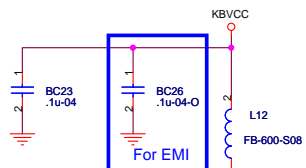
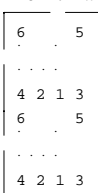




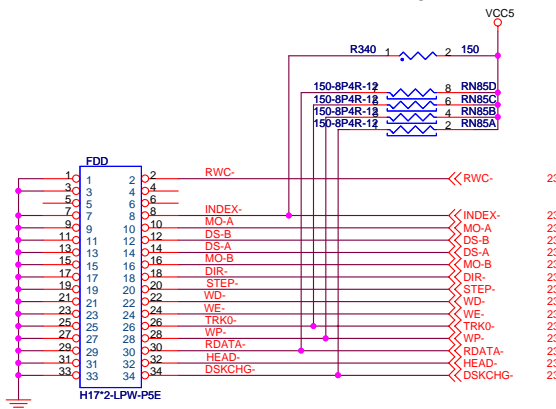
CONNECTOR VIEW



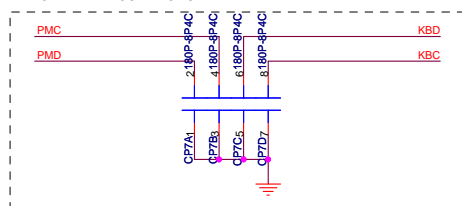
TOP VIEW



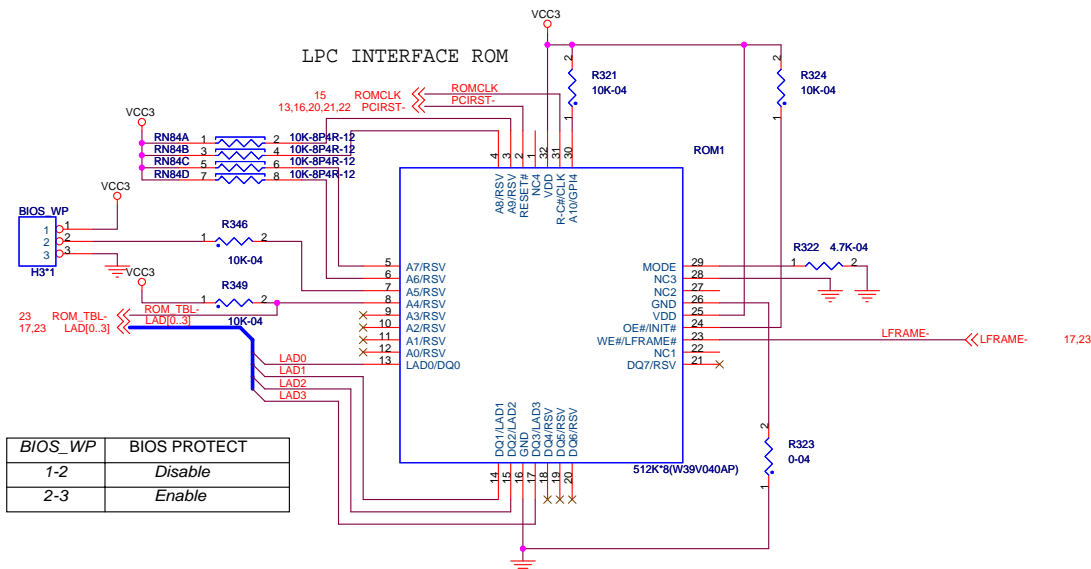
FDC



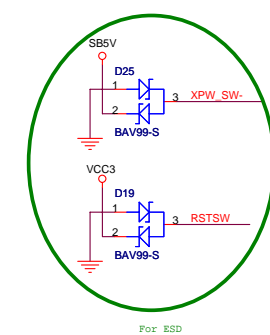
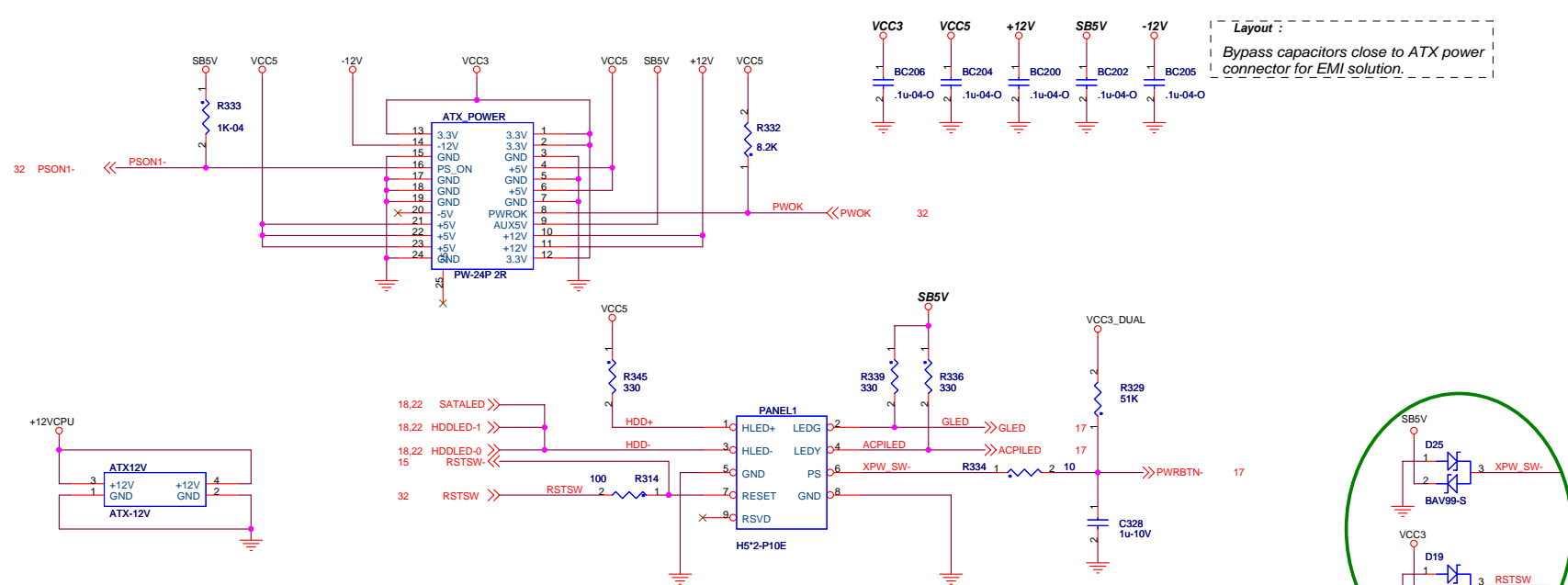
PLACE NEAR CONNECTOR



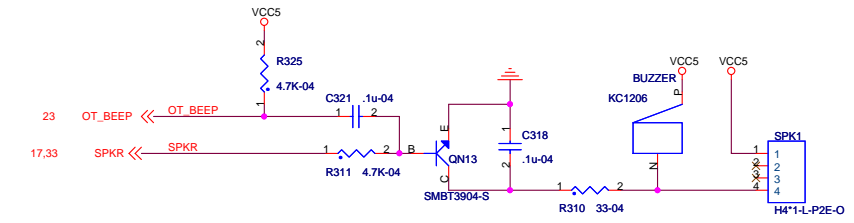
LPC INTERFACE ROM



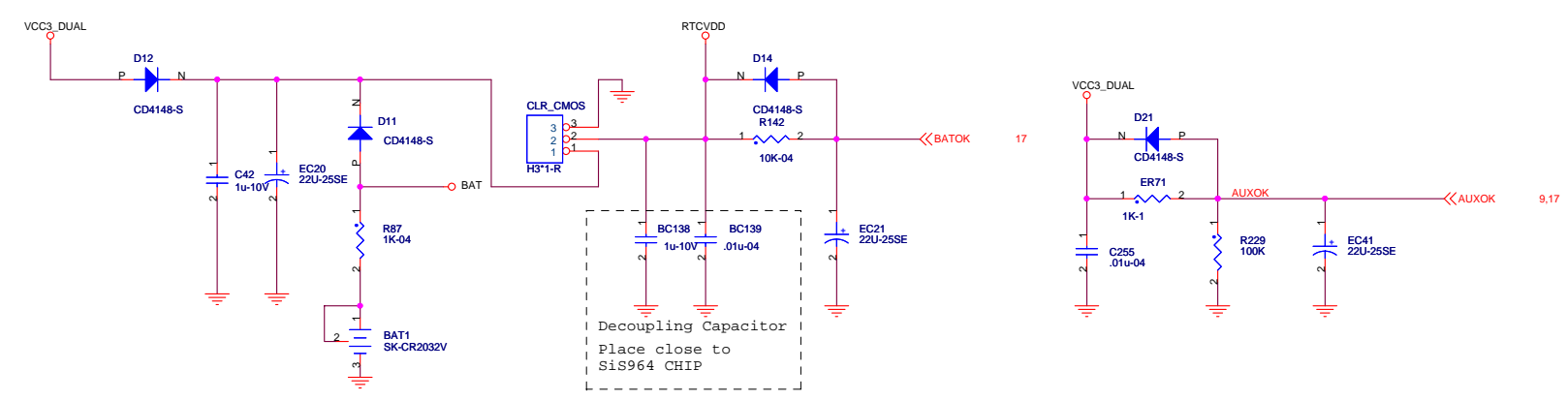
BIOS_WP	BIOS PROTECT
1-2	Disable
2-3	Enable

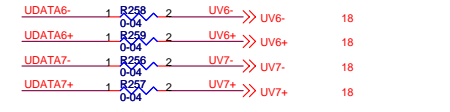
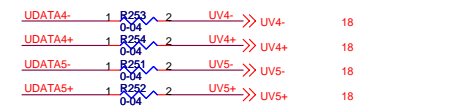
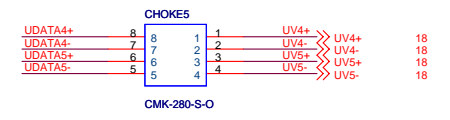
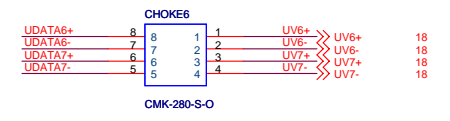
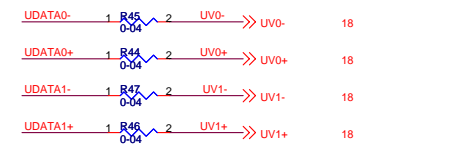
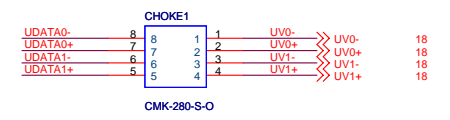
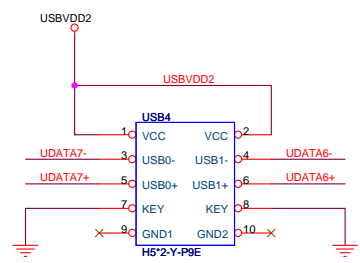
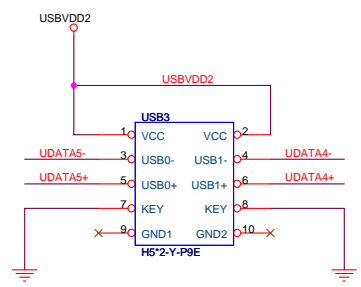
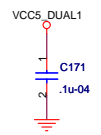
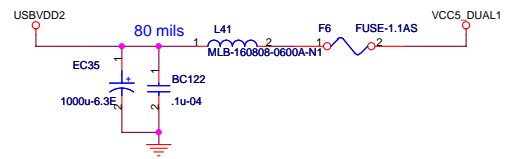
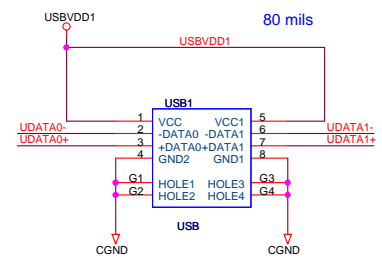
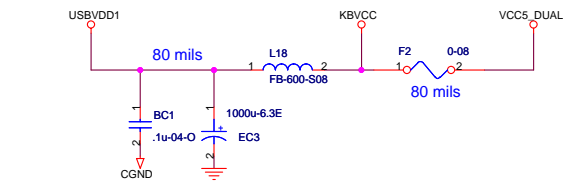


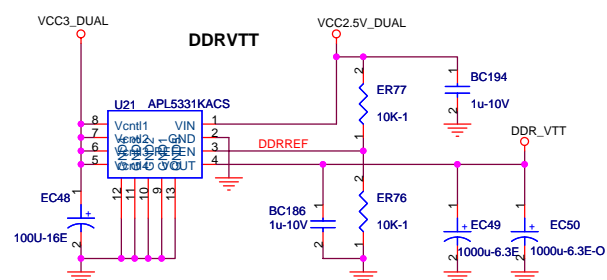
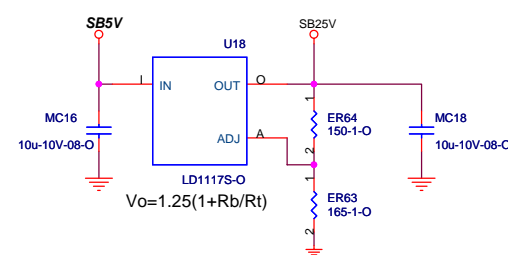
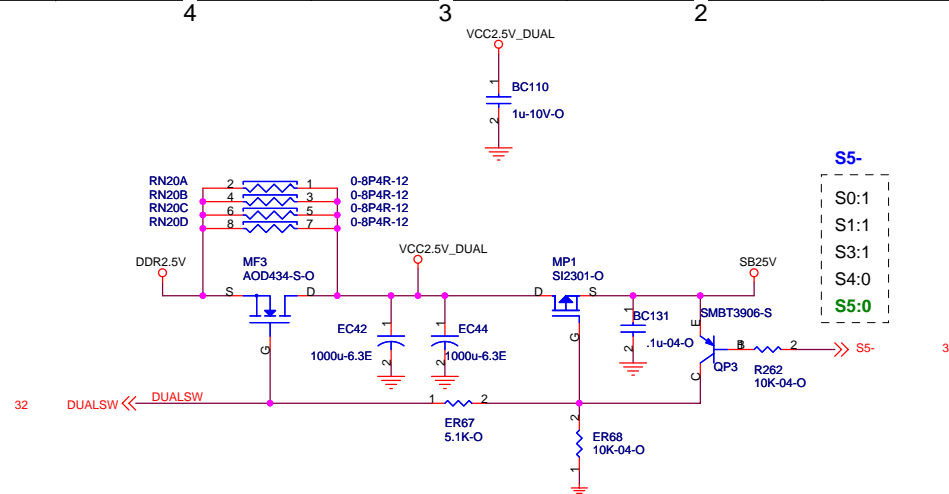
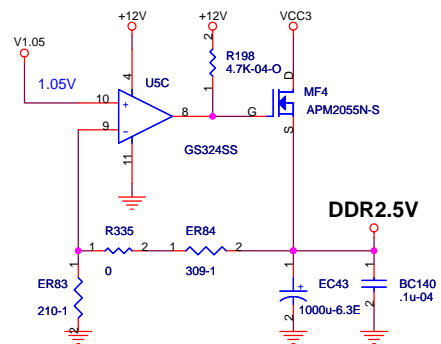
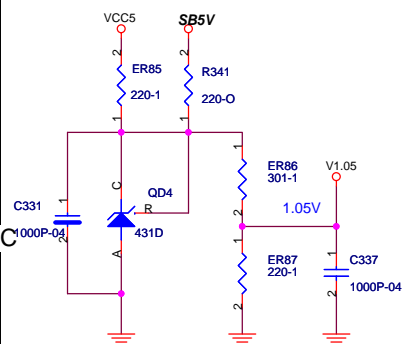
PANEL1	
HDD LED	SUS LED
1	2
3	4
5	6
7	8
9	10
RST SW	KEY PWR SW

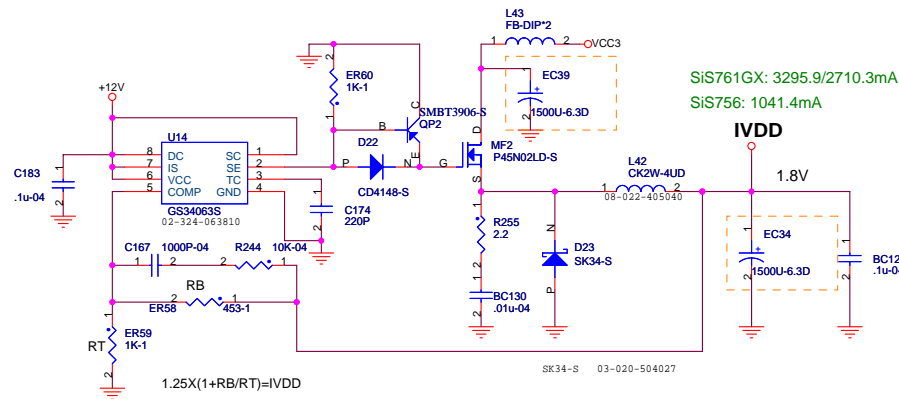


CLR_CMOS	CLEAR CMOS
1-2	Normal (default)
2-3	Clearing







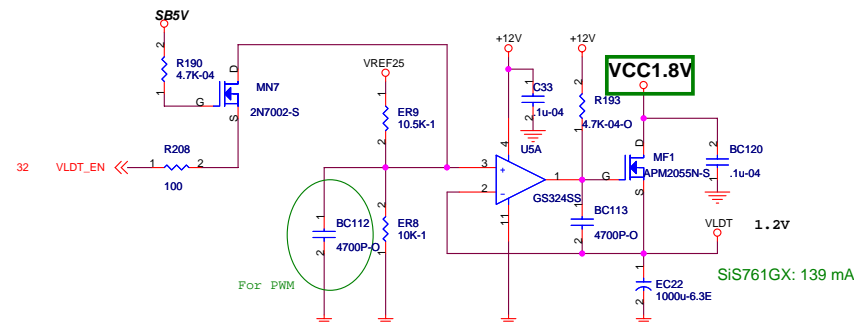
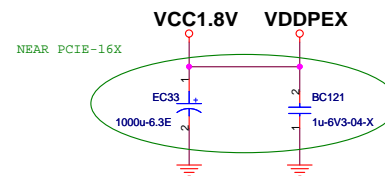
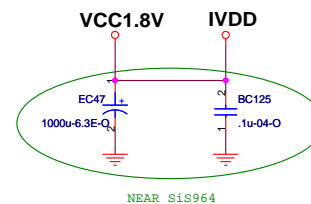
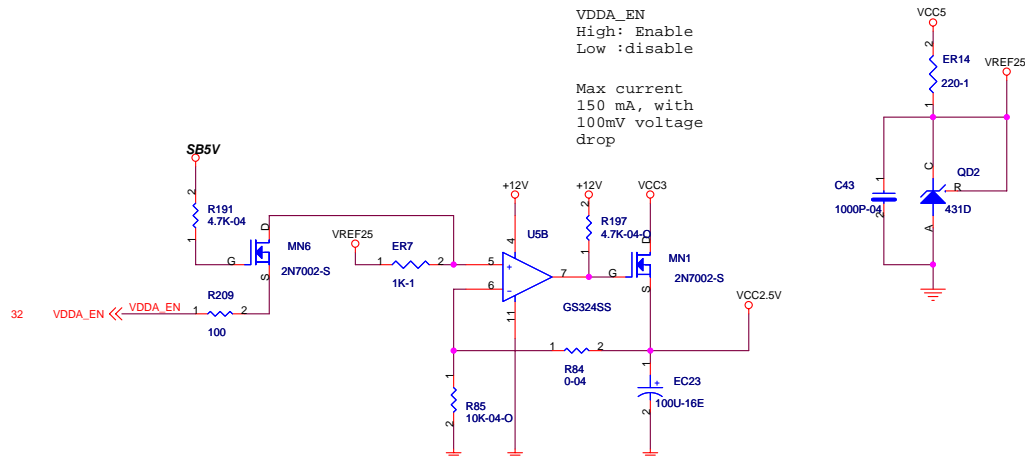


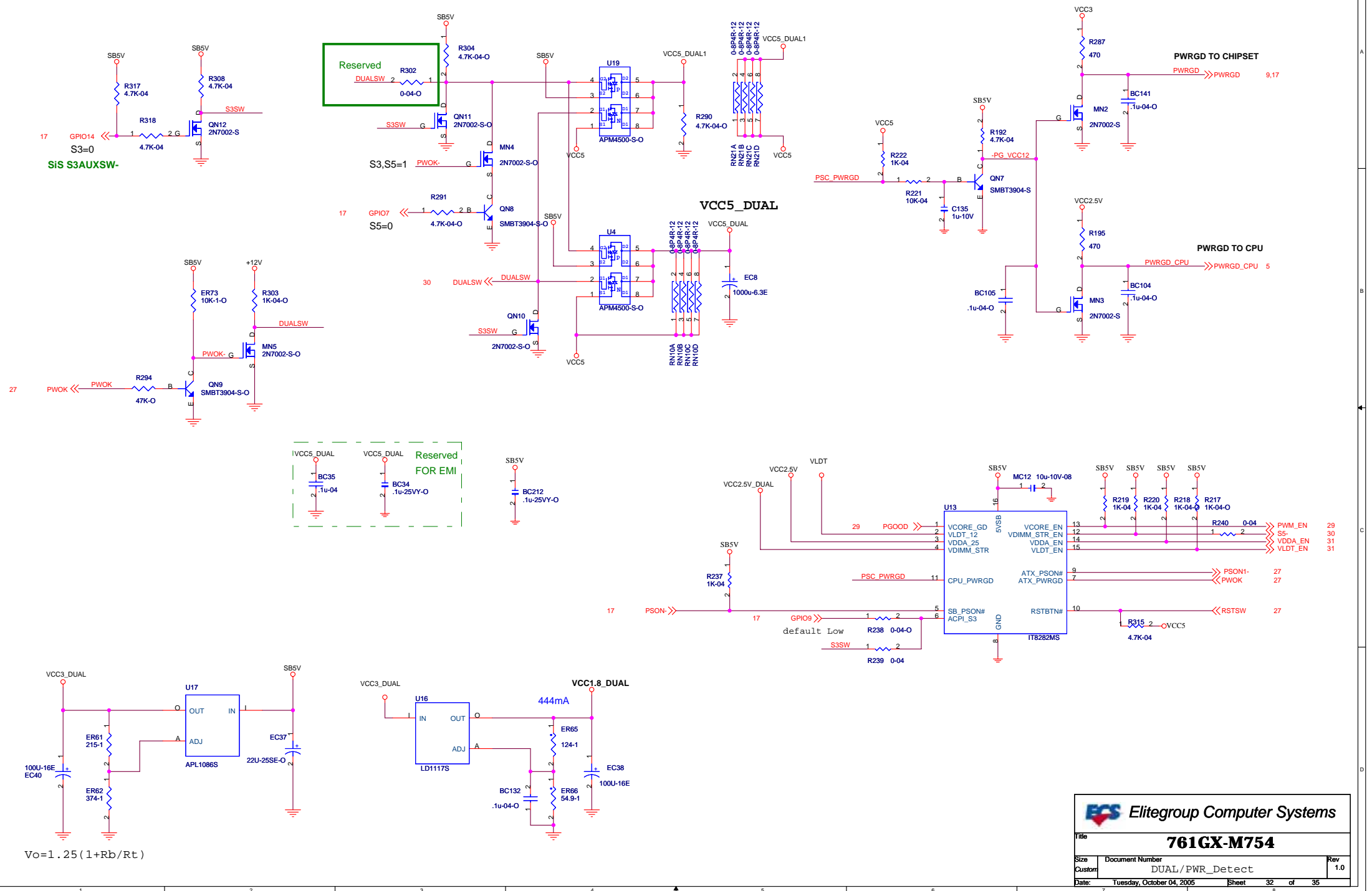
$$1.25 \times (1 + RB/RT) = IVDD$$

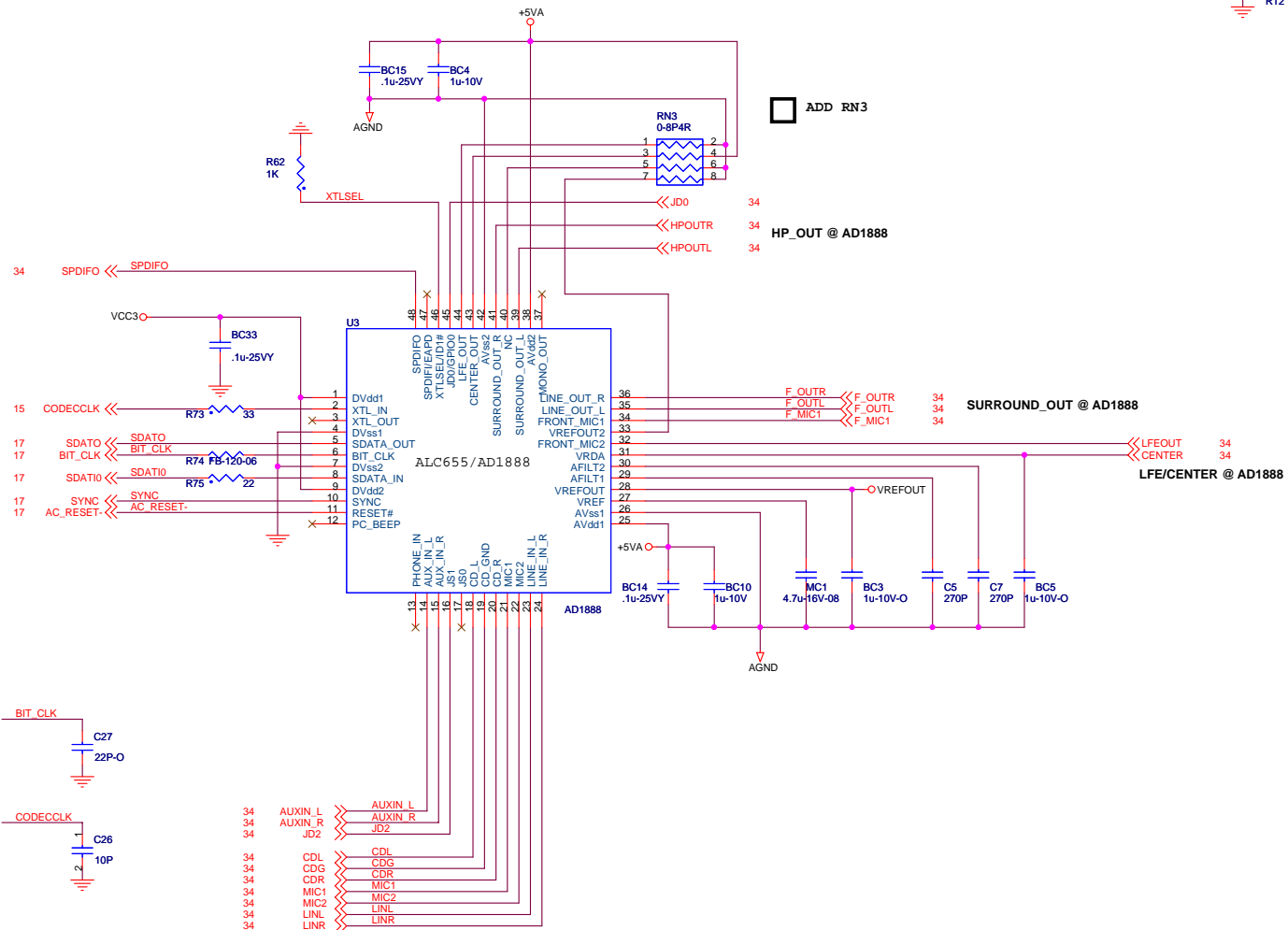
ER58 -> 487 OHM = 1.86V
ER58 -> 453 OHM = 1.81V
ER58 -> 442 OHM = 1.8V
ER58 -> 200 OHM = 1.5V

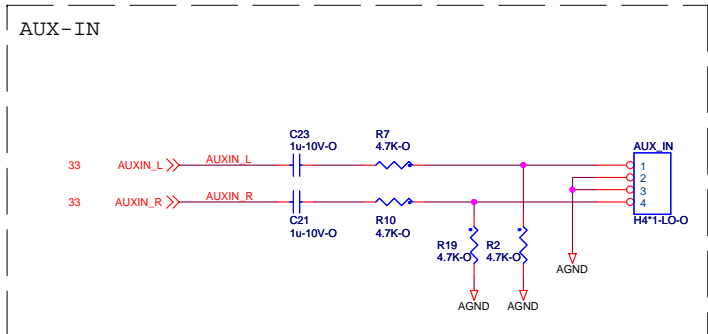
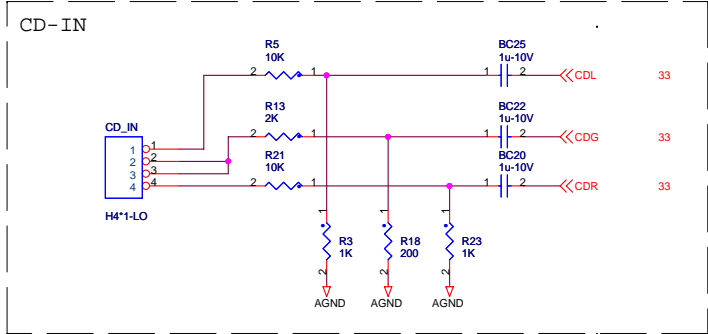
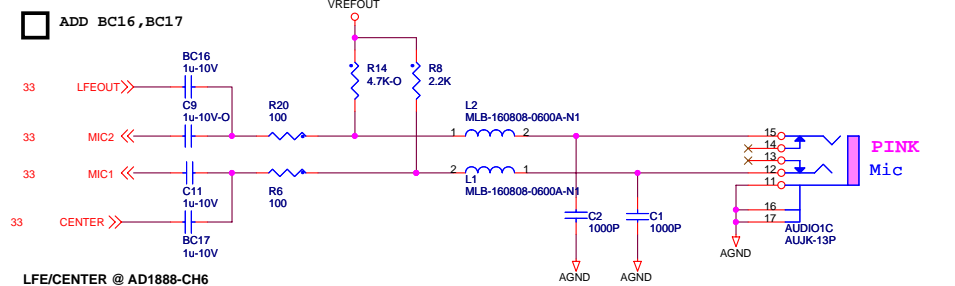
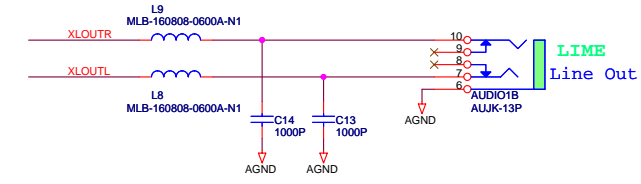
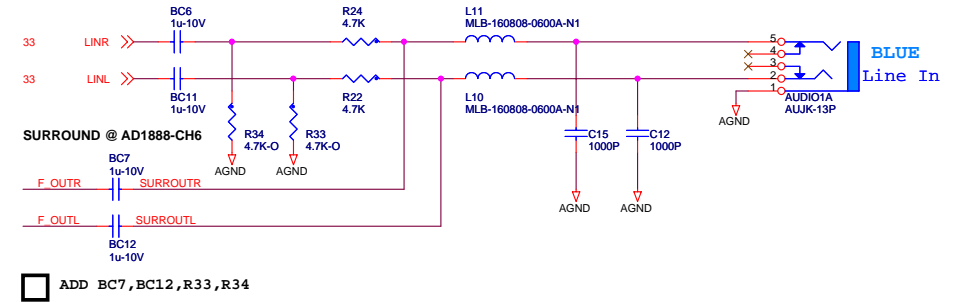
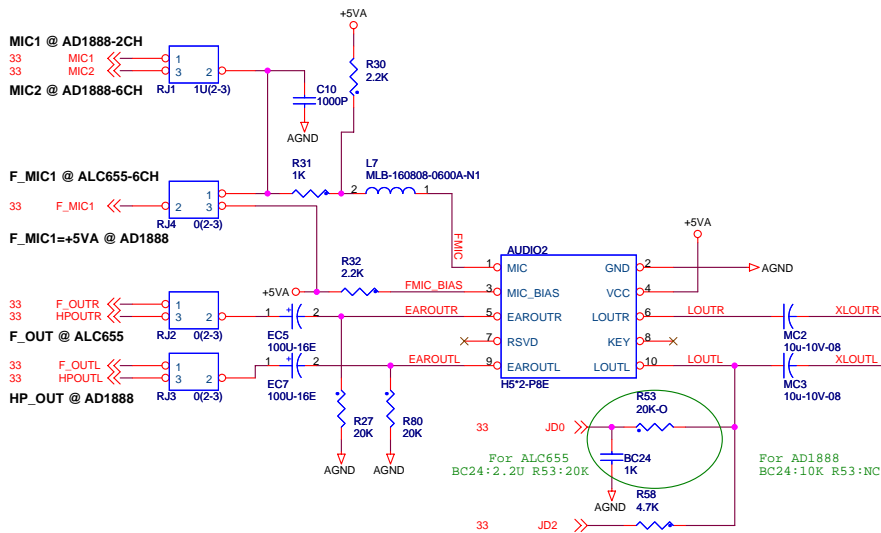
VDDA_EN
High: Enable
Low: disable

Max current
150 mA, with
100mV voltage
drop









SPDIF-Out Pin Definition1

